Switching Mechanisms, Electrical Characterisation and Fabrication of Nanoparticle Based Non-Volatile Polymer Memory Devices.

Dominic Charles Prime MEng

A thesis submitted to De Montfort University
in partial fulfilment of the requirements for the
degree of Doctor of Philosophy

Emerging Technologies Research Centre
De Montfort University, Leicester

January 2010

Declaration

I declare that this thesis has not been submitted in part or whole for any other degree or qualification at De Montfort University, or any other academic institutions.

The work contained in this thesis is as a result of my own effort unless otherwise stated.

"Science is not about building a body of known 'facts'.
It is a method for asking awkward questions and subjecting them to a reality-check,
thus avoiding the human tendency to believe whatever makes us feel good."
...Terry Pratchett

Acknowledgements

I'd like to express my gratitude to Dr Shashi Paul, head of Emerging Technologies Research Centre (EMTERC), for his expert guidance and continuing assistance. The coffee breaks have been a welcome distraction and the varied discussions we have had together were always enlightening. Thanks are also due to him for offering me the opportunity to do this PhD.

My appreciation goes to Dr Patrick Josephs-Franks for the supervision and advice provided during my research, and for the training and access to the UHV-STM equipment at NPL.

I am indebted to Mr Paul Taylor, principal research technician at EMTERC for ordering equipment, supplies and components, as well as his assistance with the various equipment used. My appreciation also goes to Dr Konstantin Vershinin for providing electric field simulation results. Thanks also go to all the students and staff members of EMTERC for help and advice when it was needed.

Thanks go to Dr Mark Green for kindly supplying the Type-I gold nanoparticles used during the research.

My sincere gratitude goes to my mum, Angela Prime for proof reading my thesis and now understanding that organic electronics doesn't mean "flowers that light up". Thanks in particular also go to Dr Andrew Wallace and Nare Gabrielyan for their advice, as well as my friends and family for their support throughout this research.

Finally I am thankful to The National Physical Laboratory (NPL) and the Engineering and Physical Sciences Research Council (EPSRC) for their financial support of my studentship.

Abstract

Polymer and organic electronic memory devices offer the potential for cheap, simple memories that could compete across the whole spectrum of digital memories, from low cost, low performance applications, up to universal memories capable of replacing all current market leading technologies, such as hard disc drives, random access memories and Flash memories. Polymer memory devices (PMDs) are simple, two terminal metal-insulator-metal (MIM) bistable devices that can exist in two distinct conductivity states, with each state being induced by applying different voltages across the device terminals.

Currently there are many unknowns and much ambiguity concerning the working mechanisms behind many of these PMDs, which is impeding their development. This research explores some of these many unanswered questions and presents new experimental data concerning their operation.

One prevalent theory for the conductivity change is based on charging and charge trapping of nanoparticles and other species contained in the PMD. The work in this research experimentally shows that gold nanoparticle charging is possible in these devices and in certain cases offers an explanation of the working mechanism. However, experimental evidence presented in this research, shows that in many reported devices the switching mechanism is more likely to be related to electrode effects, or a breakdown mechanism in the polymer layer.

Gold nanoparticle charging via electrostatic force microscopy (EFM) was demonstrated, using a novel device structure involving depositing gold nanoparticles between lateral electrodes. This allowed the gold nanoparticles themselves to be imaged, rather than the nanoparticle loaded insulating films, which have previously been investigated. This method offers the advantages of being able to see the charging effects of nanoparticles without any influence from the insulating matrix and also allows charging voltages to be applied via the electrodes, permitting EFM images to capture the charging information in near real-time.

Device characteristics of gold nanoparticle based PMDs are presented, and assessed for use under different scenarios. Configurations of memory devices based on metal-insulator-semiconductor (MIS) structures have also been demonstrated. Simple interface circuitry is presented which is capable of performing *read*, *write* and *erase* functions to multiple memory cells on a substrate.

Electrical properties of polystyrene thin films in the nanometre thickness range are reported for the first time, with insulator trapped charges found to be present in comparable levels to those in silicon dioxide insulating films. The dielectric breakdown strength of the films was found to be significantly higher than bulk material testing would suggest, with a maximum dielectric strength of 4.7 $MV \cdot cm^{-1}$ found, compared with the manufacturers bulk value of 0.2 – 0.8 $MV \cdot cm^{-1}$. Conduction mechanisms in polystyrene were investigated with the dominant conduction mechanism found to be Schottky emission.

Table of Contents

List of Figures

List of Tables

CHAPTER 0

Overview of Thesis

Organic and polymer based electronics can offer the possibility of cheap, simple electronic devices, with the potential for low temperature fabrication techniques and even the opportunity to print electronic circuitry in the future.[1-2]. The obvious application for these devices will likely be in low cost, lower performance, large area electronics, leaving conventional semiconductor devices for high performance applications. However, for certain applications there is also a need to directly compete with established semiconductor devices, such as in the area of non-volatile, rewritable memories such as hard disc drives and Flash memories. Scott [3] argues that all the current market leading memory technologies have their limitations, so there is a need for a memory which combines all the benefits of low cost, high performance and long retention times. Conventional semiconductor scaling is also rapidly approaching the fundamental limits of what is possible before the devices themselves become comparable in size to the atoms that they are constructed from [4-5]. Combining all these facts, it is clear that a fundamentally new technology, such as an organic electronic based memory device may be able to address all of these problems.

Organic and polymer memory devices (OMDs and PMDs) based on simple metal-insulator-metal (MIM) structures incorporating metal nanoparticles have been demonstrated [6-13] and in some cases show quite remarkable device characteristics. Nevertheless, there is still much debate in the scientific community regarding the exact mechanisms by which these devices are showing bistability and non-volatility. Whatever the intended application for the memories, whether it is in low performance, low cast applications, or as a universal memory as envisaged by Scott [3], until these questions are answered and any ambiguities are resolved it is unlikely that this type of memory can progress to commercialisation.

In the majority of the work published to date the PMDs are studied as a whole entity, hence the roles which the individual constituents are playing is unknown, or at best, not well understood. This is also true for the host polymer material in many PMDs, which is rarely studied and most cases has little data concerning its electrical characteristics. This research will investigate the switching mechanisms in polymer memory devices, by scrutinising the proposed working mechanisms and conducting thorough investigations into the roles of the individual components which constitute a PMD. By systematic experimentation and

objective analysis of results, experimentally backed-up theories will be proposed to explain the switching characteristics of PMDs.

0.1. Organisation of Thesis

Following this Chapter, which gives an overview of the thesis and its organisation, the remainder of the thesis is arranged as follows:

Chapter 1 gives an introduction to the two fundamental themes of the research, organic electronics and digital memory devices.

Overviews of current emerging memory technologies are described in Chapter 2, followed by a review of the literature related to organic and polymer memory devices. Missing areas of knowledge are discussed and the aims of the research outlined.

In Chapter 3 important concepts and experimental techniques are introduced, with the prominent mechanisms of electrical conduction described and the fundamental operating principals of scanning probe microscopy detailed.

Chapter 4 is concerned with thoroughly investigating the electrical properties of thin polystyrene films, including the theory behind the experiments conducted and analysis of experimental results.

Experimentation designed to investigate the theorised switching mechanisms in gold nanoparticle based polymer memory devices can be found in Chapter 5. Polymer memory devices themselves, as well as the constituent materials and appropriate test structures are all scrutinised.

In Chapter 6 device characteristics of gold nanoparticle based polymer memory devices are shown and compared with the required operating characteristics for polymer memory devices to become a viable technology. The responsible mechanisms for conductivity change are proposed, drawing on experimental evidence described in the thesis. Circuitry capable of easily interfacing with polymer memory device arrays is shown and new device configurations are demonstrated and assessed for their future potential.

Chapter 7 draws conclusions to research and provides suggestions for appropriate directions for future research in the area.

The thesis concludes with appendices containing supplemental information referenced in the appropriate section of the thesis. It also includes lists of all acronyms used and values for fundamental physical constants.

0.2. Important Outcomes of the Research

The following section highlights some of the important results and outcomes from the research.

As previously discussed, the host polymer in PMDs is rarely investigated, hence prior to the research conducted in this thesis very little information was available concerning the electrical properties of the polystyrene films used in many PMDs. Polystyrene properties, such as dielectric strength, insulator trapped charge densities and conduction mechanisms have now all been investigated. Significant differences were found between thin-film properties and the previously available bulk material properties. These differences could have implications where polystyrene is used for organic electronic applications.

High profile articles by Ouyang *et al.* [9-10] and Yang *et al*. [14] have been scrutinised and it has been found that some of the experimental evidence used in the papers cannot be relied upon to support the conclusions they make. Firstly curve fitting was used to fit a particular conduction mechanism to the current-voltage (*I-V*) characteristics of the memory device. However, in §5.4 it will be shown that this method is highly ambiguous and further data would be needed to prove a particular conduction mechanism. Secondly electrostatic force microscopy (EFM) was used to support the hypothesis of gold nanoparticle charging being responsible for the conductivity change in their memory devices. Section 5.2.4 shows their experimental results are seriously flawed as the effect of the nanoparticles cannot be isolated from the effects of the polymer matrix. Redesigned experiments are then conducted, such that it is possible to distinguish the charge storage contribution from the gold nanoparticles only.

The current levels in PMDs have been thoroughly investigated in §§5.3 – 5.4 and the reported high levels of current in many devices (references [7-10, 12, 15-17] for example), have been found to be unlikely unless some form of device breakdown or filamentary conduction is considered. High levels of current coupled with reversible switching have been shown to be possible (§5.3), but only where the switching can unambiguously be attributed to filamentary formation.

Alternative PMD structures have been fabricated and demonstrated based on metal-insulator-semiconductor structures (MIS) (§6.3), with these devices offering the advantage of being based on known mechanisms.

For the first time, simple circuitry has been developed, built and tested which is capable of interfacing with and controlling PMDs.

A novel method for the fabrication of break junctions has also been developed. Previous methods have utilised comparatively complicated photolithography steps and careful monitoring of current passing through a forming break junction as electromigration occurs [18]. The method demonstrated in this research allows quick and easy fabrication of nanometre sized gaps between electrodes without the need for photolithography steps, or computer current monitoring.

0.3. Peer Reviewed Published Work and Conference Presentations

1. *"The Future's Organic: Small Molecule and Nanoparticle Based Polymer Memory Devices"*, D. Prime and S. Paul, Set for Britain 2006 Physics meeting, House of Commons.
2. *"Making Plastic Remember: Electrically Rewritable Polymer Memory Devices"*, D. Prime and S. Paul, Materials Research Society Symposium Proceedings. San Francisco, Vol 997, pp 21 – 25, 2007.
3. *"Electrical and Morphological Properties of Polystyrene Thin Films for Organic Electronic Applications"* D. Prime and S. Paul, International Materials Research Congress (IMRS) Proceedings, Cancun, S19-P26, p38, 2007.
   Full paper will appear in Vacuum (in press) - doi:10.1016/j.vacuum.2009.10.033
4. *"Gold Nanoparticle Based Electrically Rewritable Polymer Memory Devices"*, D. Prime and S. Paul. Conferences International Materiaux Technologies (CIMTEC), Sicily, 2008. Proceedings published in Advances in Science and Technology. Vol 54, pp 480 – 485, 2008.
5. *"Electrical Properties of Nanometre Thin Film Polystyrene for Organic Electronic Applications"* D. Prime, P.W. Josephs-Franks and S. Paul. IEEE Transactions on Dielectrics and Electrical Insulation. Vol. 15, No. 4, pp 905 – 909, 2008
6. *"Overview of Organic Memory Devices"* D. Prime and S. Paul. Philosophical Transactions of the Royal Society A. Vol. 367 · No. 1905, pp 1441-1448, 2009.
7. *"Gold Nanoparticle Charge Trapping and Relation to Organic Polymer Memory Devices"* D. Prime, S. Paul and P. W. Josephs-Franks. Transactions of the Royal Society A. Vol. 367 · No. 1905, pp 4215-26, 2009.
8. *"First Contact - Charging of Gold Nanoparticles by Electrostatic Force Microscopy"* D. Prime and S. Paul. Accepted for publication in Applied Physics Letters.

9. *"Storing Bits in Nanoparticles – Use of Gold Nanoparticles in Non-volatile Electrically Re-writable Polymer Memory Device"* D. Prime, M. Green and S. Paul. Submitted to Nanotechnology.

CHAPTER 1

Introduction to Organic Electronics and Digital Memories

In this chapter an introduction is given to the motivations behind the use of organic and polymer electronic materials and devices. The concept of a digital memory is then introduced along with a discussion of the current major memory technologies and their limitations, finishing with the justifications for the ongoing research into new memory technologies.

1.1. Background to Organic Electronics

The 1922 Nobel Prize winning physicist Niels Bohr [19] is attributed as saying "Technology has advanced more in the last thirty years than in the previous two thousand. The exponential increase in advancement will only continue…" Considering Bohr died in 1962 his foresight into the advancements that took place in the second half of the 20th century and are continuing into the 21st century is still remarkably accurate. At the time of his death the field of modern electronics was still in its infancy, with only 15 years passing since the demonstration of the first transistor at Bell Laboratories in 1947 [20]. However, it is the subsequent explosion in electronics and the use of integrated circuits (IC) in general that has allowed many technological advances to take place. Semiconductor devices have undergone vast improvements during this time. In fact a humorous quote of unknown origin that is incorrectly associated with Bill Gates states that "If GM [General Motors] had kept up with technology like the computer industry has, we would all be driving $25 cars that get 1,000 miles to the gallon."[21]. Despite the quotation being fictitious, it does highlight the developments that have taken place in regards to the following:

- Reduced semiconductor node size, leading to higher packing density.
- Reduced power consumption per transistor.
- Increased speed of operation.
- Improved reliability and robustness.
- Reduced costs.

However when working with conventional semiconductors, the material purities that must be achieved and the level of complexity that modern ICs posses, mean that while huge

advances have been made in all the above areas, to carry on making advances requires huge investments in fabrication facilities and ever more complex fabrication methods. Currently leading fabrication facilities are manufacturing semiconductor devices using a 45 nm process [22-23], with the next generation 32 nm process due to start before the end of 2009 [24-25]. These processes are actually ahead of the predictions made by the International Technology Roadmap for Semiconductors (ITRS) [5] and if advances continue at these rates, then fundamental scaling limits could be reached in under a decade [4].

As the cost and complexity of conventional semiconductors has increased, one promising area that has come under investigation as an alternative basis for electronic components is organic materials. This class of materials generally includes compounds based on carbon and hydrogen, and frequently includes elements such as oxygen and nitrogen, meaning that all plastic and polymer materials are included in the category. For many decades polymer materials were rigidly regarded as insulators, with their main use in electronic circuits being confined to insulators on wires, or as encapsulation materials to prevent environmental ingress into circuits. However, in 1977 Heeger, MacDiarmid and Shirakawa *et al*. [26] discovered that the conductivity of polyacetylene could be altered by up to 13 orders of magnitude upon doping, spawning the field of conducting and semiconducting polymer materials.

Polymer materials and polymer based electronics have the benefit of offering the following advantages over conventional inorganic semiconducting materials:

- Low cost of materials.
- Low cost fabrication techniques due to low temperature deposition and processing.
- Simpler fabrication steps and less stringent purity requirements.
- Large area fabrication techniques such as materials printing or roll-to-roll processes.
- Flexibility. Fabrication on a large variety of substrates, including flexible plastic substrates for foldable or highly robust devices.

Due to their future potential, tremendous research efforts have been undertaken in the field of polymer electronics, with significant advancements made and demonstrations of devices such as organic light-emitting diodes (OLED) [27], thin film transistors [2] and solar

cells [28]. There are also a limited number of commercially available devices starting to be released, mainly in the area of digital displays, such as the first commercial OLED television, Sony's XEL-1 [29].

1.2. Introduction to Digital Memory

The world today is increasingly reliant on information and the ability to be able to access that information wherever we are, at whatever time we want. In fact it is hard to imagine being without the electronic devices that connect us, not only with each other, but also with the World Wide Web. To reflect the reliance on, and the ability to manipulate information the term "information age" has been used by some to describe this highest level of technological advancement that has been achieved. Electronic devices are prolific in this information age, with even the most mundane of objects containing electronic circuitry (musical greeting cards for example). Underlying all of this technology is the modern integrated circuit, and inevitably wherever there is a circuit with some processing capability, there will also be digital memory present.

So what exactly is meant when the term digital memory is used? Figure 1.1 shows diagrammatically the characteristics of a digital memory and defines the terms that will be used throughout this investigation.

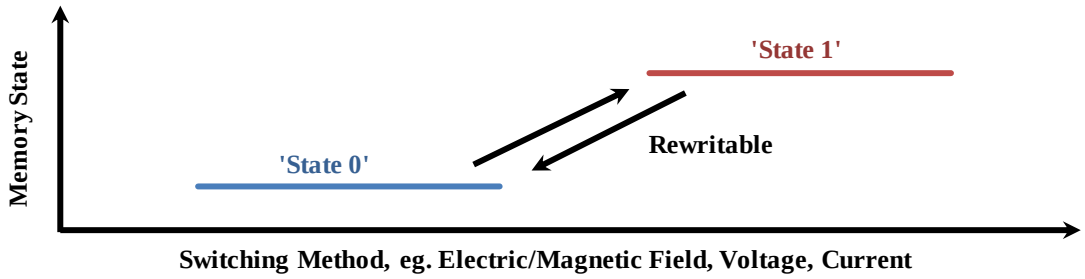


Figure 1.1 Schematic illustration of a digital memory.

At its most fundamental level digital memory needs to show bistable behaviour in order to be able to store either a '1' or a '0'. Secondly there are two other characteristics that define what class of memory the device falls into; namely rewritability and volatility. A rewritable memory is one which can be switched repeatedly between its two states (as indicated by the arrows in Figure 1.1) for many cycles without degradation in memory performance. A non-volatile memory is one which also retains its state when no source of electrical power is applied, while a volatile memory looses the stored information once the power is disconnected. This also introduces the concept of a memory cycle, with one cycle being

defined as switching the memory from one state to the other and back again. The final memory characteristic that will be used is the speed of the memory. Here, different memory operations usually have different speeds, with *read*, *write* and *access* speeds being the most commonly quoted. *Read* and *write* speeds are the approximate time taken to read or write an individual bit of data respectively, while the *access* time is the time taken to initially access the first bit of data. In some memory technologies (especially hard disc drives and Flash) there is also an asymmetry between the *read* and *write* performances, with the *read* performance usually 2x or 3x faster than the *write* speeds.

Currently the memory market is dominated by three main types of memory; dynamic random access memory (DRAM), hard disc drives (HDD) and Flash memory. Each technology has its own advantages and disadvantages, with DRAM competing favourably in terms of shear performance due to fast speed (~10^{-9} s *read/write/access*) and high number of cycles (10^{15}). It also has the advantage of being a relatively simple design, so high memory densities are possible. It does have the disadvantage of being a volatile memory though, so requires a constant power source. Hard disc drives offer the greatest storage density at the lowest cost (currently a few pence per gigabyte [30]), a high number of cycles (10^{12}) and indefinitely long retention time, however, it is also the slowest technology (10^{-8} s *read/write*, 10^{-2} s *access*) and can suffer from mechanical failures. Flash memory has the advantage of being non-volatile, with good retention times (> 10 years), however it still doesn't compete with DRAM in terms of performance, with moderate speeds (10^{-8} s *read/write*, 10^{-3} s *access*) and moderate cycles (10^{6}). Due to the complicated cell structure and the number of processing steps required in manufacture, flash was traditionally the most expensive of the three memory architectures, however prices have fallen considerably within the last two years. With current prices of approximately one pound per gigabyte [31] flash is now starting to be able to compete with HDDs in some high performance applications [32].

In 2004 Scott [3] argued that there was a need for a ubiquitous, or universal memory that combined the benefits of all three memories, i.e. fast access times, high number of cycles, long retention times and low cost. At the time, flash memory was prohibitively expensive as a serious alternative and despite the fall in price of flash memory, it still has inherent performance issues that mean it will never be able to compete with DRAM in terms of performance. Without the prospect of any of the current memory technologies being able to offer all of the characteristics that would be required for a true universal memory there has been a great deal of research conducted into emerging memory technologies.

Currently there are several technologies that show some promise, including:

- MRAM – Magnetoresistive Random Access Memory.
- FeRAM – Ferroelectric Random Access Memory.
- PCRAM – Phase-Change Random Access Memory.
- NRAM – Nano Random Access Memory.
- Racetrack Memory.
- RRAM – Resistive Random Access Memory.

Each of these memory technologies will be briefly outlined and discussed in the following chapter.

CHAPTER 2

Overview of Emerging Memory Technologies and Review of the Current Status of Organic Memory Devices

"The powers of technology appear to be unlimited. If some of the dangers may be great, the potential rewards are greater still"

...Donald. S. L. Cardwell

Dictionary of the History of Ideas, 1973

In this chapter an overview will be given of the emerging memory technologies that are vying to become universal memories, which ideally should offer all the benefits of fast access times, high number of cycles, long retention times and low cost.

Comparisons between the different classes of organic memory devices that have been investigated by others will then be given, describing the general structure of the devices and the characteristics they exhibit.

A comprehensive review of the work conducted in the field of OMDs and PMDs then follows, with the roots of the field originating approximately 50 years ago, through to the latest research conducted and the large increase in interest in the field over the course of the past decade.

2.1. Current Emerging Memory Technologies

2.1.1. MRAM – Magnetoresistive Random Access Memory

Magnetoresistive-RAM is based on memory cells containing two magnetic storage elements, one with a fixed magnetic polarity, while the second has a switchable polarity. These elements are positioned on top of each other and separated by a thin insulating tunnel barrier as shown in the cell structure in Figure 2.1.

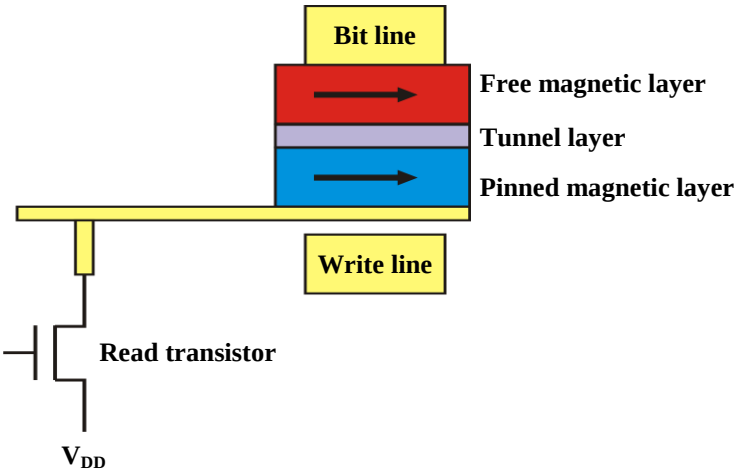


Figure 2.1 Basic MRAM cell structure.

The state of the cell is sensed by measuring the electrical resistance when passing a current through the cell. Due to the magnetic tunnel effect [33] if the two magnetic moments are parallel to each other, then electrons will be able to tunnel and the cell is in the low resistance *on* state. However, if the magnetic moments are anti-parallel then the cell resistance will be high. Writing and erasing are performed by passing a current though the *write* line to induce a magnetic field across the cell.

Currently MRAM has reached some level of commercial success [34] in niche applications. Companies such as IBM, Toshiba, Samsung and Hitachi among others are actively developing MRAM chips, or variant technologies of MRAM. In terms of power consumption and speed MRAM competes favourably with other memories such as DRAM and Flash, with access times of a few nanoseconds demonstrated [35], however, the minimum cell size may be limited by the spread of the magnetic field into neighbouring cells during the *write* operation. The price of MRAM is also currently a limiting factor, with prices far in excess of all the currently established memories, at approximately £2-3 per megabyte [36]. At these pricing levels MRAM is in excess of 1,000 times the price of Flash memory and over 10,000 times the price of hard disc drives. While the price may drop as more companies release MRAM chips it seems unlikely that it will ever be able to compete competitively as a universal memory.

2.1.2. FeRAM – Ferroelectric Random Access Memory

Ferroelectric-RAM shares some similarities with the layout of a DRAM cell, consisting of a capacitor and transistor structure. The cell is then accessed via the transistor which enables the ferroelectric state of the capacitor dielectric to be sensed.

In a DRAM cell the data periodically needs refreshing due to the discharging of the capacitor, whereas the FeRAM maintains the data without any external power supply. It achieves this by using a ferroelectric material in the place of a conventional dielectric material between the plates of the capacitor. When an electric field is applied across a dielectric or ferroelectric material it will polarise. When that field is removed the dielectric will depolarise. However, the ferroelectric material exhibits hysteresis in a plot of polarisation versus electric field and will retain its polarisation. One disadvantage of FeRAM is the fact that it has a destructive *read* cycle. The *read* method involves writing a bit to each cell, if the state of the cell changes then a small current pulse is detected indicating the cell was in the *off* state. However, FeRAMs can endure a high number of cycles ($\sim 10^{14}$) [37], meaning that the requirement for a *write* cycle for every *read* cycle will not result in short product lives.

FeRAM has also achieved a level of commercial success, with the first devices released in 1993 [38]. Current FeRAM chips offer performance that is either comparable to, or exceeding current Flash memories [37, 39], but which is still currently slower than DRAM. Again with FeRAM, price is an issue at approximately £2-3 per megabyte [40], meaning once again, many orders of magnitude improvement would be needed before FeRAM could compete as a universal memory.

2.1.3. PCRAM – Phase-Change Random Access Memory

Phase-Change RAM is based on a class of material called chalcogenide glasses that can exist in two different phase states (i.e. crystalline and amorphous). Each of these states has different conductivity properties and hence can be used as the basis of a non-volatile memory. These materials are in fact commonly used as the data layer in rewritable compact discs and digital versatile discs, (CD-RW and DVD-RW) where the change in optical properties is exploited to store data. In this application the phase of the chalcogenide glass is altered by localised heating due to the laser pulses, while in a PCRAM a current is passed through the glass to heat it and change its phase. This process has been demonstrated to be on the order of a few tens of nanoseconds [41], potentially making it comparable to Flash for the

read operation, but several orders of magnitude faster for the *write* cycle. Data retention times of >10 years are projected, and importantly a high number of *write* cycles can be applied to the memories before they fail [42]. Possible problems facing PCRAM concern the high current density needed to erase the memory, however, as cell sizes decrease the current needed will also decrease. Production of PCRAM was announced recently by both collaborations between Intel and STMicroelectronics [43], and Samsung [44], though pricing information is currently unavailable.

2.1.4. NRAM – Nano-Random Access Memory

Nano-RAM is a carbon nanotube (CNT) based memory, which works on a nanomechanical principal, rather than a change in material properties [45]. Produced by Nantero [46] these memories consist of the structure shown in Figure 2.2(a) with an array of bottom electrodes covered by a thin insulating spacer layer. CNTs are then deposited on the spacer layer, leaving them freestanding above the bottom electrodes. Unwanted CNTs are removed from the areas around the electrode, with top contacts and interconnects deposited on top of the patterned CNT layer. When the CNTs are freestanding there is no conduction path between the bottom and top electrode and hence the memory cell is in the *off* state. However if a large enough voltage is applied over the cell the nanotubes are attracted to the bottom electrode where they are held in place by Van der Waals forces. Due to the conductive nature of the CNTs the electrodes are now connected and the cell reads the low conductivity *on* state (Figure 2.2(b)). The *off* state can be returned by repelling the nanotubes with the opposite electrode polarity. Non-volatility is achieved due to the strength of the Van der Waals forces overcoming the mechanical strain of the bent nanotubes, hence holding the cell in the *on* state. NRAM offers the possibility of a simple cell architecture, that could operate at much higher speeds than conventional flash and with lower power usage. However, as NRAM is based on CNTs it suffers from the fabrication problems that are inherent in carbon nanotube based devices. These issues include; cost and fabrication complexity of producing the CNTs, ensuring uniform dispersions of nanotubes and difficulties in removing nanotubes from the unwanted positions on the substrate.

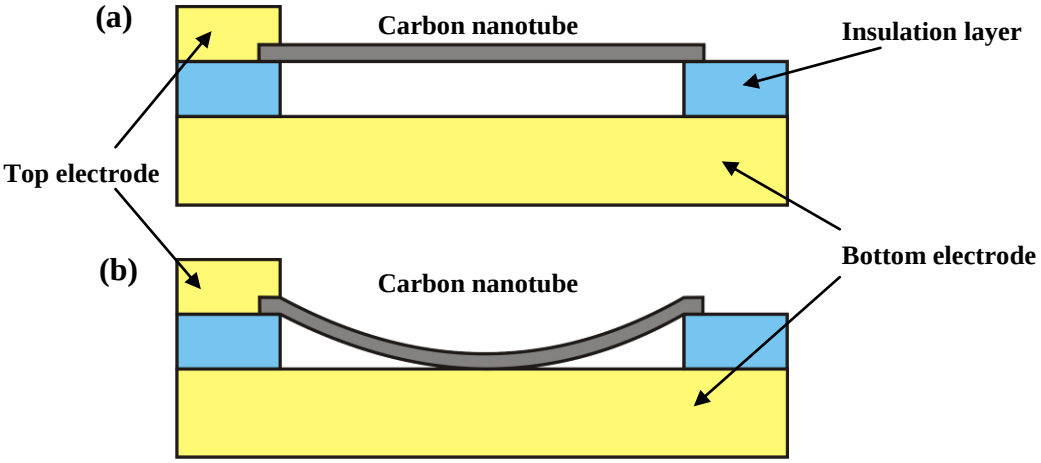


Figure 2.2 NRAM memory structure. (a) Off state. (b) On state.

2.1.5. Racetrack Memory

Racetrack memory [47-48] in some respects is technologically similar to conventional hard disc drives, in that it also stores data in magnetic domains. However in racetrack memory the magnetic information is stored in domains along nanoscale permalloy wires. The magnetic information itself is then 'pushed' along the wire, past the *read* and *write* heads by applying voltage pulses to the wire ends. In this way the memory requires no mechanically moving parts, hence has a greater reliability and higher performance than HDDs, with theoretical nanosecond operating speeds [48]. For a device configuration where data storage wires are fabricated in rows on the substrate, conventional manufacturing techniques are adequate. However, for the maximum possible memory density the storage wires are proposed to be configured rising from the substrate in a 'U' shape, giving rise to a 3-dimensional forest of nanowires. While this layout does allow high data storage densities, it also has the disadvantage of complex fabrication methods, with so far, only 3-bit operation of the devices demonstrated [49]. As the access time of the data is also dependent on the position of the data on the wire, there would also be performance losses if longer wires are used to increase the storage density further. The speed of operation of the devices has also been an issue during development, with much slower movement of the magnetic domains than originally predicted. This has been attributed to crystal imperfections in the permalloy wire [50] which inhibit the movement of the magnetic domains. By eliminating these imperfections data movement speeds of 110 $m \cdot s^{-1}$ have been demonstrated [50].

2.1.6. RRAM – Resistive Random Access Memory

Resistive RAM architectures potentially offer the simplest cell structure of any of the emerging memory technologies, with a simple crossbar structure of electrodes either side of a resistive film. The film can exist in one of two conductivity states, which can be induced by applying voltage pulses to the electrodes. Many different inorganic and organic insulators have been used as the resistive material, with fast switching times on the order of 10 ns demonstrated in modern RRAMs [51-52]. RRAM in many respects shows similarities with many of the memory devices that are reviewed in §2.3, hence a full review of the structure, mechanisms and materials will be given in the sections which follow.

2.2. Types of Organic Memory Devices

It is possible to characterise the organic memory devices that have so far appeared in publications and literature into one of three broad categories:

- Resistive switch and *write once, read many times* (WORM) devices.
- Molecular memory devices.
- Polymer memory devices.

It should however be understood that these categories are by no means exclusive of each other, with large grey areas between them where some demonstrated devices can fall into two (or possibly even all three) categories.

This work is primarily concerned with polymer memory devices, and hence this will be the field covered in much greater detail during reviews of previous work published. However, due to the large overlaps an understanding of the developments in other related fields of organic memories is also important, as some of the mechanisms that govern how these devices work could be pertinent when studying the characteristics of PMDs. Brief descriptions of the different types will firstly be discussed in §§2.2.1 – 2.2.3, broadly illustrating the differences between the memory types, with the detailed reviews of previous work following in §2.3.

2.2.1. Resistive Switch and WORM Devices

These devices potentially offer the simplest device structure, consisting of a cross point array of top and bottom electrodes, separated by a resistive material as shown in Figure 2.3. Each place where the top and bottom electrodes cross is one memory cell.

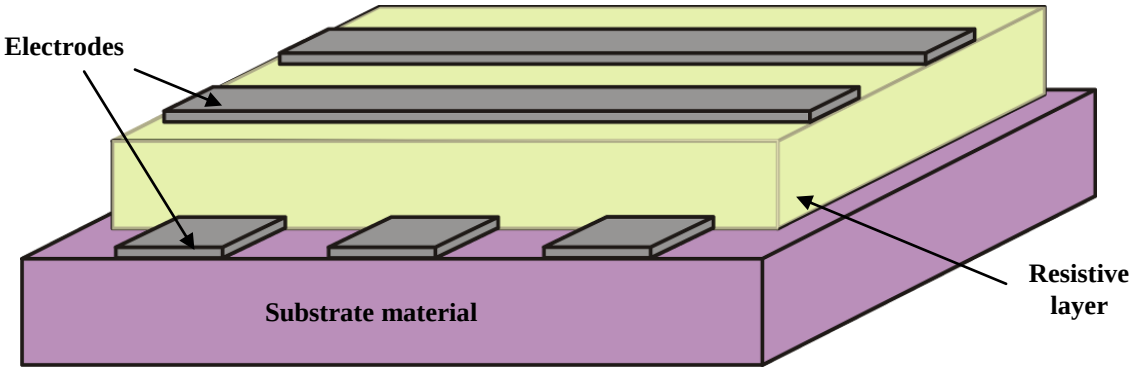


Figure 2.3 Structure of a resistive switch memory device.

Depending on the material that the resistive layer consists of, it can change in one of two ways when a voltage pulse is applied across the cell. The first type of device will short circuit between electrodes, giving a lower resistance than the pristine state, the second type acts like a blown fuse, giving a higher resistance than the pristine device.

2.2.2. Molecular Memories

In a molecular memory a monolayer of molecules is sandwiched between a cross point array of top and bottom electrodes as shown in Figure 2.4. The molecules are packed in a highly ordered way, with one end of the molecule electrically connected to the bottom electrode and the opposite end of the molecule connected to the top electrode. Langmuir-Blodgett (LB) deposition is ideally suited for depositing the molecular layer in these devices.

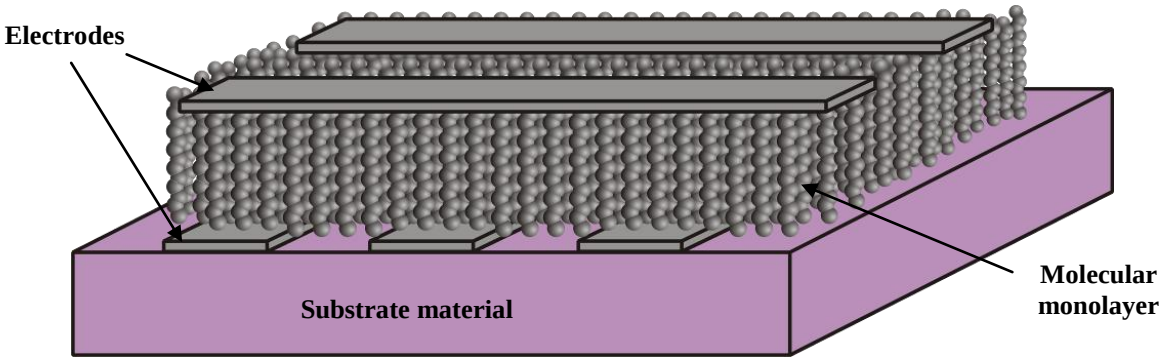


Figure 2.4 Structure of a molecular memory device.

By applying a voltage between the electrodes the conductivity of the molecules is altered, enabling data to be stored in a non-volatile manner. The process can then be reversed and the data erased by applying a voltage of the opposite polarity to the memory cell.

2.2.3. Polymer Memory Devices

Polymer memory devices also consist of a layer of organic material sandwiched between a cross point array of top and bottom electrodes. In this structure the organic layer consists of an admixture of deliberately introduced molecules and/or nanoparticles in an organic polymer matrix, as illustrated in Figure 2.5.

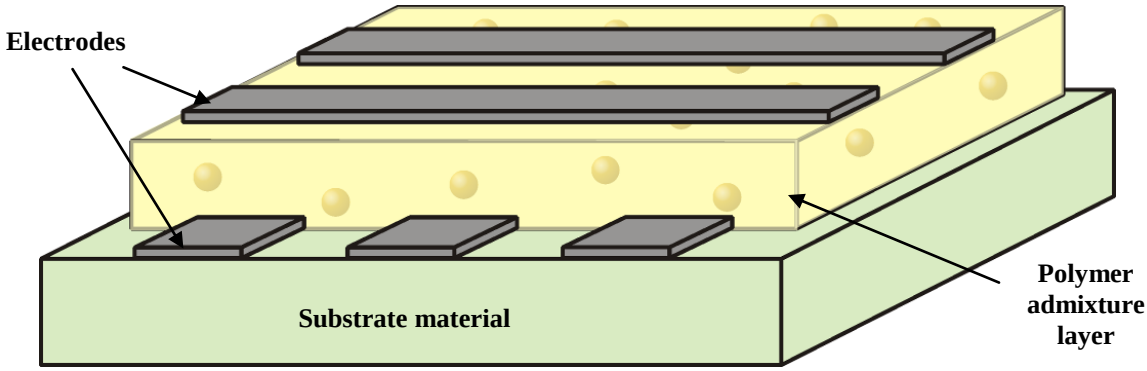


Figure 2.5 Structure of a polymer memory device.

Deposition of the organic layer is usually done by the spin-coating method. All the required constituent materials are dissolved in a solvent which is then spun onto the substrate. As the solvent evaporates a thin film of material in the region of tens to hundreds of nanometres thick is deposited on the bottom layer of electrodes. Top electrodes are deposited as the final step.

The conductivity of the organic layer is then changed by applying a voltage across the memory cell, allowing a bit of data to be stored.

2.3. Previous Work Done in the Field of Organic and Polymer Memory Devices

2.3.1. Current - Voltage Characteristic Shapes

Before an in depth discussion of previous work is undertaken, it is prudent to add a brief description of the general shapes that have been reported in the current-voltage characteristics of organic memory devices, this will allow the reader to visualise the descriptive terms used. In the majority of OMDs and PMDs the bistability of the devices is demonstrated by investigating the *I-V* characteristics, which shows that for a given *read* voltage there exists two different conductivity states and hence two different current responses. The bulk of *I-V* characteristics published so far can be grouped into one of three general shapes, namely, N-shaped, S-shaped and O-shaped.

N-shaped characteristics (illustrated in Figure 2.6) are typified by a low current up to a certain threshold voltage (V_T) (region 1), where a sudden increase in current by up to several

orders of magnitude becomes apparent (region 2). If the voltage is then reduced, the device stays in this high conductivity state and has a high current response (region 3). However, if voltages higher than V_T are applied a phenomena known as *negative differential resistance* (NDR) occurs, here an increase in voltage leads to a reduction in current (region 4). Voltages higher than the NDR region once again return the device to its low conductivity state. These devices respond symmetrically to applied voltage, so applying negative voltages has the same effect as positive voltages.

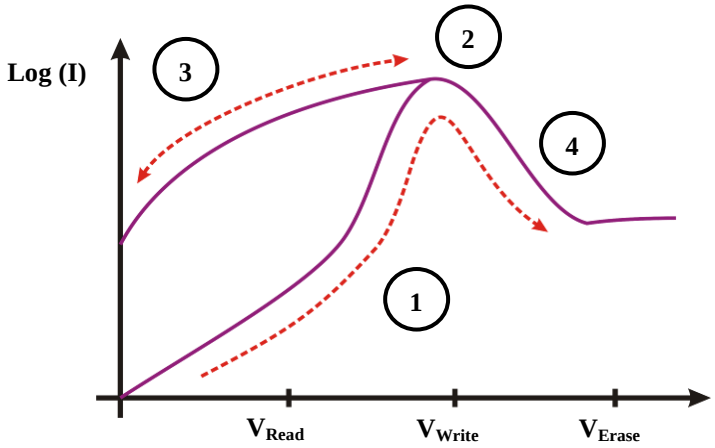


Figure 2.6 N-shaped current-voltage characteristic.

S-shaped *I-V* characteristics are similar to N-shaped characteristics with respects to the sudden increase in current at a voltage V_T, however these plots do not show the NDR region, but instead current continues to increase with applied voltage. Both symmetric and asymmetric characteristics are possible, with symmetric devices (Figure 2.7(a)) switching to the *on* state with a V_T of either polarity. Some devices revert to the *off* state when the voltage is reduced to zero, making them volatile memories. In others only a very small voltage of the opposite polarity is needed to switch the devices off. With asymmetric devices, shown in Figure 2.7(b), the *on* state is maintained when the voltage is reduced, while a negative voltage is needed to switch back to the low conductivity state.

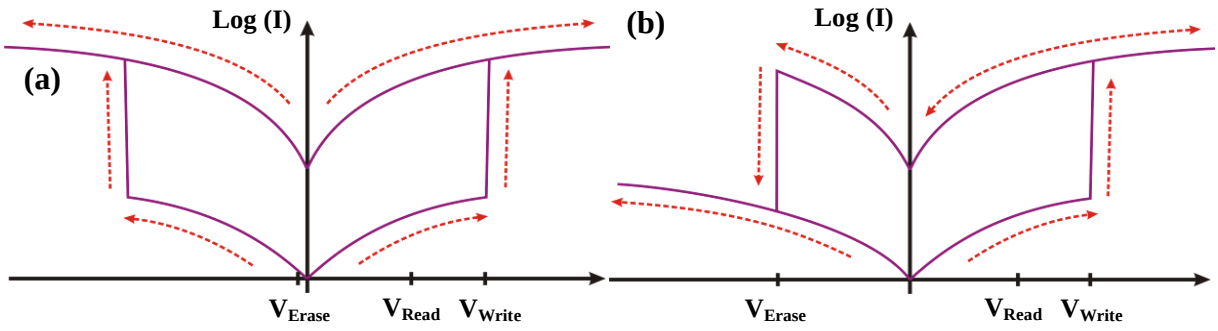


Figure 2.7(a) Symmetric S-shaped and (b) Asymmetric S-shaped current-voltage characteristics.

The final type, O-shaped characteristics, do not show any abrupt increase in current at a specific voltage, but instead show a simple hysteresis loop. Figure 2.8 demonstrates this showing an anticlockwise hysteresis loop for a positive applied voltage, however, this loop can also be clockwise, i.e. the write voltage can either increase or decrease the conductivity, depending on the device studied.

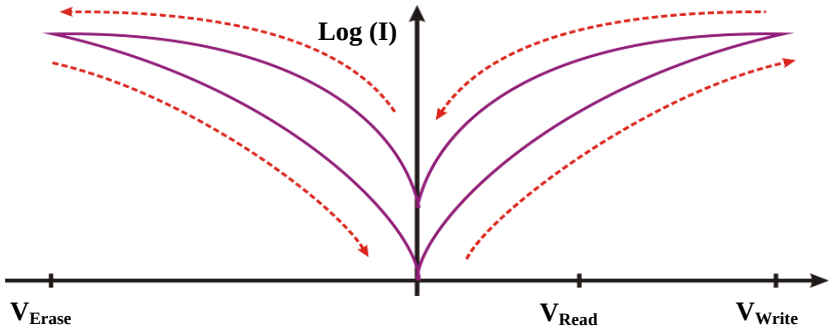


Figure 2.8 O-shaped current-voltage characteristic.

2.3.2. Resistive Switch and WORM Devices

The field of organic memories is considered to be relatively new, with high profile articles popularising the field only appearing within the past 5 years [3]. However, the origins of the work date back to the early 1960's, when thin films of insulating materials were shown to exhibit electrical switching, and in most cases regions of NDR.

The phrase *forming*, or the now more common *electroforming* came into use to describe the process by which the insulating material's conductivity is altered when a voltage above a certain threshold voltage is applied. Initially the insulating materials investigated were inorganic insulators such as Al_3O_2 [53-55], SiO [56], ZnS [57] and TiO [58], organic and polymeric insulators were also soon investigated and found to exhibit similar electroforming behaviour [59-60]. However, there was still much uncertainty over the mechanisms that were responsible, theories include:

1. Metal ion injection from the electrodes, leading to impurity bands in the insulator [56].
2. Conducting filamentary pathway formation due to electrolytic processes [55].
3. Formation of filaments from either the metallic electrodes [57, 60-61], carbonaceous material from the insulator itself, or from sources introduced during manufacture of the devices [62-63].

4. Tunneling between metal islands produced during the electroforming process [64].
5. Oxygen atom motion in oxide insulating films [65].

The majority of papers published which attempt to explain the phenomena observed in electroformed metal-insulator-metal claim that filamentary formation occurs in the insulating material, forming a low conductance pathway between the electrodes [57, 60-62, 66-68]. However despite multiple efforts to image filaments using various microscopy techniques, such as scanning electron microscopy (SEM), transmission electron microscopy (TEM) [69] and scanning tunneling microscopy (STM) [66, 70-71] there is still only circumstantial evidence for their existence. Pagnia *et al*. [70] concluded that if filaments existed, they could be no larger than the resolution of the STM being used.

Despite the devices ability to function as electronic memory elements and the proponents of using the devices as such, resistive switching devices have been regarded by several as unsuitable for non-volatile memory applications. This is due to the large areas of uncertainty in their operation and the possibility that the mode of operation is actually due to a physical breakdown of the device [64, 72].

One exception to this is when a device is being intentionally and irreversibly damaged to change the state of a memory cell, as is the case with WORM devices. Forrest *et al*. demonstrated a WORM device based on a polymer fuse of PEDOT [73]. The as-deposited device shows high conductance due to the conducting polymer PEDOT, but when a sufficiently high voltage is applied across the memory cell the polymer fuses burn causing a low conductance state.

Applications for this type of device are limited to replacements for programmable read only memories (PROMs), where data doesn't need to be rewritten, meaning the market is much more limited than for a rewritable bistable device.

As discussed in §2.3.1 any device showing a NDR region has a general N-shaped characteristic, as is the case for all the bistable resistive switches discussed here. It is therefore likely that similar (if not the same) mechanisms are responsible despite the differences in materials used.

2.3.3. Molecular Memories

The first devices to appear in publication that were claimed to work via electrical switching in monolayers of oriented molecules between two metallic electrodes were

demonstrated by Chen *et al*. [74] in 1999. He demonstrated that a benzene based molecule containing amine and nitro groups could exhibit bistability, concluding that the change in conductivity was due to a two step reduction process in the molecule. The first reduction supplies an excess electron, providing a charge carrier for electron flow and hence high conductivity. If the voltage is increased a second reduction step takes place, this blocks the current flow in the system and leads to low conductivity. Similar results were obtained by Reed *et al*. [75], who demonstrated that molecules without the nitro group did not show switching behaviour. Retention times of >15 minutes were possible and multiple memory cycles were shown, however no mention of the ultimate number of memory cycles is given.

Subsequent papers by Chen *et al*. [76-77] demonstrated that the memory effect was also present at the nanoscale, by fabricating 40nm^2 memory cells. These papers were also the first to present data regarding statistical analysis of devices, highlighting variations from 10 to 10^4 for *on/off* ratios. Typical *on/off* ratios of 100 were reported, but quickly decayed to unity after a few hundred cycles at most. Also 50% of devices only switched once, those that did show rewritable behaviour had large variations in switching voltages, ranging from 3.5 to 7V. Overall, out of 24 8x8 matrices analysed only three showed no catastrophic defects, which emphasises the need for improvements in these devices before viable memories can be achieved.

Other molecules including DDQ [78], TAPA [78] and Rose Bengal [78-80], have been demonstrated to exhibit bistability. All research groups have found that the prerequisite for bistability is that the molecule possesses groups that can be chemically reduced when a voltage is passed through them, allowing the mechanisms described by Reed *et al*. [75] to take place.

Despite the majority of research groups claiming that reduction/oxidation mechanisms are responsible for the switching in these organic memories, there are still some uncertainties, with another possible mechanism being filament formation. Jakobsson *et al*. [81] conducted systematic experiments on Rose Bengal molecular devices, finding that switching only occurred in a small area of the device with an associated heat spot at that position. He concluded that switching was due to repeatable formation of conductive filaments.

The main problem with molecular devices has been found to be the variability between them, with large differences in characteristics being present, even between devices on the same substrate. This could be a symptom of having a large number of molecules present, with even a nanoscale device having ~1100 molecules for a 40 nm^2 area [77].

2.3.4. Polymer Memory Devices

In some respects many of the devices which fall into the polymer memory device category could be included in the resistive switch category. This is especially true of the devices which consist solely of a polymer layer sandwiched between electrodes. In many cases they show remarkably similar behaviour to those classed as organic resistive switches. Despite the similarities in characteristics, and even in some cases similar proposed mechanisms for the switching phenomenon, the authors themselves do not class their work as resistive switches and also no longer use the term electroforming in relation to the switching. For this reason, most modern devices studied (year 2000 onwards) will be classed as PMDs.

The first device based on this structure was studied by Ma *et al*. [6] and consisted of a polymer derivative of anthracene called MDCPAC, in a sandwich structure between gold and aluminium electrodes. By applying various voltages to the devices the MDCPAC layer conductivity could be changed, resulting in a non-volatile, bistable memory device. It was proposed that the mechanism for the change in conductivity was trap sites in the polymer film being filled when an electric field was applied, but no conclusive evidence was presented and the performance of the devices as memory elements was not discussed. It was also noted that the gold bottom electrode was crucial for switching to take place, with no switching occurring when aluminium bottom electrodes were used.

The next progression in devices came from structures first proposed by researchers at the University of California, Los Angeles (UCLA) [7-8, 82-85]. This consisted of a tri-layer structure of organic/metal-nanocluster/organic sandwiched between two aluminium electrodes (named as 3-layer organic bistable devices - 3L-OBDs). AIDCN, an organic semiconducting polymer was used for the organic layers. The metal-nanocluster layer was formed in these devices by evaporating a thin metal layer in the presence of oxygen or AIDCN, forming discontinuous metal-nanoclusters. It was proposed that charge could be stored at either side of the nanocluster layer thereby doping the AIDCN layers and significantly increasing the conductivity of the devices, allowing bits of information to be stored. Many permutations of metals [7] and various layer thicknesses [85] were studied with *on/off* ratios in the devices ranging from 4 – 6 orders of magnitude, depending upon the structure studied. In [84] He *et al*. showed that switching mainly occurs in the bottom organic layer, postulating that this was due to the organo-metallic complex formed by evaporating the top contact, giving rise to an asymmetric device structure. It is also shown in this paper that

devices can be made symmetric by deliberately introducing an Al_2O_3 layer under the top electrode. However, this casts doubts over the mechanisms discussed, as Al_2O_3 was one of the first materials found to show resistive switching and could be playing an important role in the switching mechanism itself. All of the devices based on nanocluster layers [7-8, 82-83, 85] were symmetric S-shaped devices, showing no NDR region, apart from [84] which showed asymmetric S-shaped characteristics.

Similar structures have also been fabricated by Bozano *et al*. [13] with the mechanisms for bistability being investigated in greater detail and also relating electrical characteristics to those found in electroformed MIM diodes, concluding that similar mechanisms were likely to be responsible for the two memory states. Despite supposedly the same structure being investigated, Bozano *et al*. found NDR to be present in the devices, leading to symmetric N-shaped characteristics and highlighting that characteristics can also be as much dependent upon the research group, as on the device structure. Subsequent investigations by Tondelier *et al*. [86] studied the same 3L-OBD structure as well as devices without the middle metal-nanocluster layer (calling them 1L-OBDs) and found that similar switching behaviour was present even without the middle metal layer. They concluded that metal nanoparticles were included in the polymer layer due to the thermal evaporation of the top electrode, with metallic filaments of nanoparticles forming in the polymer under high electric fields, giving rise to a high conductivity *on* state.

A subsequent evolution in device structure came by including ready made nanoparticles in the devices, rather than relying on nanoparticles forming during fabrication of the devices. Paul *et al*. [87] demonstrated the first of these devices by incorporating a monolayer of gold nanoparticles via the Langmuir-Blodgett technique into the insulating layer of metal-insulator-semiconductor capacitors. Capacitors including nanoparticles were found to show hysteresis in their capacitance-voltage characteristics when compared to devices without nanoparticles. This was attributed to electrons being injected onto the nanoparticles from the gate electrode, charging the nanoparticles and allowing data storage. Similar results were also demonstrated in MIS structures more recently by Leong *et al*. [88], however they attributed the hysteresis as being due to holes injected onto the nanoparticles. While the devices demonstrated in these papers were not used directly as PMDs, they demonstrated that the principle of using nanoparticles as charge storage elements was feasible.

The first paper to integrate discrete nanoparticles into MIM memory structures was presented by Ouyang *et al*. [9] who demonstrated that devices with discrete nanoparticles

would behave in a similar manner to the metal-nanocluster devices previously studied by Ma *et al*. [7-8, 82-83, 85]. Devices comprised of an admixture of gold nanoparticles capped with dodecanethiol (termed Au-DT in the report. These nanoparticles are also the same as the Type-II nanoparticles used during this research) and 8-hydroxyquinoline (8HQ) molecules in a polystyrene matrix. It has been shown that 8HQ and gold nanoparticles can act as electron donors and acceptors respectively [89-91], with the change in conductivity in these devices attributed to the transfer of electrons from the 8HQ molecules to the Au-DT. This positive and negative charging of the 8HQ and Au-DT respectively leads to a change in the conduction properties of the insulating film. A tunneling mechanism between 8HQ molecules was proposed as being responsible for the high conductivity *on* state with a combination of Fowler-Nordheim and direct tunneling being fitted to the experimental data. Further evidence for the charge transfer between 8HQ and Au-DT devices was presented in the form of EFM images of the polymer layer, without the top electrode. By biasing the film with positive and negative voltage with the EFM probe, the different conductivity states could be induced and then sensed by scanning over the whole area at a *read* voltage. The images presented showed pronounced EFM signals between the different pre-biased areas of the substrate. The significance of these particular experiments will be discussed fully in §5.2.4.1.

Ouyang *et al*. [16] later studied MIM structures including nanoparticles capped with 2-naphthalenethiol (Au-2NT) embedded in a polystyrene matrix. Here the proposed mechanism was a transfer of electrons from the capping ligands of the nanoparticles and the nanoparticle core itself, with tunneling between the nanoparticles responsible for the conduction in the *on* state. These devices were found to only exhibit WORM characteristics with no transition back to the *off* state.

Work on investigating the effect of nanoparticles based on different metals, as well as the position of the nanoparticles in the structure and electrode material has been carried out by Bozano *et al*. [12]. Bistability was shown to be a common phenomenon among the materials chosen and the structures investigated. All devices here used semiconducting organic material as the organic layers of the device, with compositions similar to those studied in [7] and [9]. However, once again Bozano *et al*. reported N-shaped *I-V* characteristics, in disagreement with those of Ma *et al*. [7] and Ouyang *et al*. [9-10, 16] who in all cases reported S-shaped characteristics. Bozano *et al*. found that characteristics were broadly similar to those reported by Simmons and Verderber (SV) [56] in their work on electroformed MIM structures and concluded that similar conduction mechanisms are

responsible. The main differences being that in the SV model Au atoms introduced from the electrodes create charge transport and trapping sites in the insulator, here, that role is played by the gold nanoparticles. Hence conduction in the *on* state is dominated by tunneling between the nanoparticles.

Devices based on gold nanoparticle and 8HQ admixtures have also been investigated by Prime *et al*. [92-93]. In these devices O-shaped characteristics were reported, with no abrupt transition between *on* and *off* states.

Other structures based on gold nanoparticle charge transfer complexes have also been studied with P3HT [94], PVK [95] and PCm [15] being used as both the electron donor material, and the polymer matrix material. Similar S-shaped characteristics were reported in all the papers, however Prakash *et al*. [94] reported that the *on* state current fitted well with Poole-Frenkel emission, based on field enhanced thermal emission of trapped charges, rather than the tunneling mechanism widely reported in other papers. Reddy *et al.* [96-97] found Poole-Frenkel emission to the dominant in the *off* state in devices based on aluminium nanoparticles, while *on* state current fitted Fowler-Nordheim tunneling.

In order to ensure nanoparticles were well dispersed in the devices Tseng *et al*. [98] incorporated platinum nanoparticles into the tobacco mosaic virus (TMV), finding that bistability only occurred when the nanoparticles were present, with the mechanism again being attributed to charge transfer, this time between the TMV and the nanoparticles.

Table 2.1 summarises the main findings of papers based on metal nanoclusters and metal nanoparticles.

Table 2.1 Summary of metal nanocluster and nanoparticle PMDs

Device structure	*I-V* shape	Switching mechanism	Memory Performance	Ref
Al/AIDCN/Al/AIDCN/Al	S-shaped	Polarisation of middle Al nanocluster layer	*On/off* ratio: 10^6	[7]
Al/AIDCN/Al/AIDCN/Al Al/AIDCN/Cu/AIDCN/Al Al/AIDCN/Au/AIDCN/Al Al/Alq3/Al/Alq3/Al	S-shaped	NOT due to metallic filaments	*On/off* ratio: 10^6	[82]
Al/AIDCN/Al/AIDCN/Al	S-shaped	Trapped charges / polarisation in the middle metal layer	*On/off* ratio: 10^4 Retention: several weeks Cycles: > 1 million Switching time: 10 ns	[83] [84]
Al/AIDCN/Al/AIDCN/Al	S-shaped	Polarisation of middle Al nanocluster layer	*On/off* ratio: 10^3 Retention: > 3hours Cycles: > 10,000	[85]

Al/Alq3/Al/Alq3/Al	N-shaped	SV mechanism – charge trapping in metal nanoclusters	Not discussed	[13]
Al/pentacene/Al	S-shaped	Metallic pathways of nanoparticles. Ohmic behaviour in *on* state.	*On/off* ratio: 10^9 Retention: > 1 week Cycles: > 100	[86]
p-Si/$Si0_2$/Au-NP/CdAA/Al	-	Charge trapping of electrons on gold nanoparticles	Not discussed	[87]
n-Si/$Si0_2$/Au-NP/pentacene/Al	-	Charge trapping of holes on gold nanoparticles	Not discussed	[88]
Al/Au-DT+8HQ+PS/Al	S-shaped	Charge transfer between 8HQ and Au-DT. *On* state: Tunneling between 8HQ molecules	*On/off* ratio: 10^4 Cycles: > 5 Switching time: < 25 ns	[9] [10]
Al/Au-NT+PS/Al	-	Charge transfer between ligand and Au-NT core. *Off* state: electrode limited current injection *On* state: space-charge limited current	*On/off* ratio: 10^3 Retention: > 60 hours	[16]
MIM structures with various electrode metals, nanoparticle metals and polymer matrices.	N-shaped	SV mechanism – charge trapping in metal nanoclusters. *On* state: tunneling between metal nanoparticles	*On/off* ratio: 10-10^6 Dependant as much on the device, than the difference between structures.	[12]
Al/Au-NP+8HQ+PS/Al	O-shaped	Charge transfer between 8HQ and Au-NP.	*On/off* ratio: 10 Cycles: ~50 Retention: > 3 hours Working devices ~90%	[92] [93]
Al/Au-NP+P3HT/Al	N-shaped	Charge transfer between P3HT and Au-NP. *Off* state: Contact limited Schottky emission *On* state: Bulk limited Poole-Frenkel emission	*On/off* ratio: 10^3 Cycles: >3000	[94]
Al/Au-NP+PVK/Al	S-shaped	Charge transfer between PVK and Au-NP.	*On/off* ratio: up to 10^5 Cycles: ~50 Retention: > 5 days	[95]
Al/Au-NP+PCm/Al	S-shaped	Charge transfer between PCm and Au-NP.	*On/off* ratio: 10^2 Cycles: > 150 Retention: ~10 hours	[15]
Al/TMV-Pt+PVA/Al	S-shaped	Charge transfer between TMV and Pt nanoparticles. *On* state: Fowler-Nordheim tunneling between Pt nanoparticles.	*On/off* ratio: > 10^3 Cycles: ~400	[98]

Another device structure to appear in publication consists of similar admixture structures to the nanoparticle devices, but utilise buckminsterfullerene (C_{60}) as an electron accepting material in place of the metallic nanoparticles. First introduced by Kanwal *et al*. [99] at the

fall Materials Research Society conference in 2004 these devices also show the required characteristics for bistability and non-volatility. Subsequent devices studied by Majumdar *et al*. [100], showed that depending upon the concentration of C_{60} the devices either exhibited bistability, or at higher concentrations WORM characteristics. Latest reports on these devices by Paul *et al*. [101] expanded on the work of Kanwal *et al*. These were the first to show that bistability was also present at the nanoscale by using a conducting atomic force microscope (c-AFM) probe as the top electrode of the device. While current difference between the *on* and *off* states at the nanoscale were significantly smaller than at the macro scale, this work did prove that high density memories could be fabricated while still retaining memory functionality.

Another memory structure demonstrated by Ma *et al*. included copper ions introduced into an AIDCN layer [102]. This device switched to a high conductivity state at approximately 0.7 V, and switched off again at 2 V. Ma *et al*. proposed that electric field induced migration of the Cu^+ ions into the polymer layer causes metallisation of the polymer layer resulting in a high conductivity state. At higher voltages the ions drift all the way across the polymer layer, returning it back to an insulator. Current ratios of 3 orders of magnitude have been demonstrated with this structure.

Other devices studied, but so far receiving less attention include memories based on Europium based charge transfer polymers [103], polymers with sulphur impurities [104], and functionalised carbon nanotubes [105].

2.4. Missing Areas of Knowledge and Research Objectives

Despite continued research and many papers being published on the subject there is still much speculation over the exact mechanisms that are responsible for the large change in conductivity that is present in many polymer memory devices. The main theories which have so far been postulated are:

- Charge transfer creating internal electric fields. This internal electric field then either enhances or diminishes an external voltage applied to the device thereby giving either high or low conductance.
- Nanoparticle/nanocluster charging leading to a change in material properties. Various conduction mechanisms have been proposed including space charge limited current, Poole-Frenkel emission, Fowler-Nordheim, or direct tunneling.

- Filamentary formation between electrodes. Conductive filaments are formed under electrical stress from either migration of electrode material, or alignment of nanoparticles. These filaments can then be ruptured returning the device to a low conductivity state.

Until the working mechanism is understood in greater detail this is likely to prove a large obstacle in the development and possible commercialisation of PMDs.

In the majority of work published to date bistability, *on/off* ratio and non-volatility are reported, which constitutes the absolute minimum requirements for a device to be called a memory. Other important device characteristics such as retention times and memory cycles before failure are either omitted completely or show large discrepancies in the reported values. This lack of data regarding longer term memory performance could be a symptom of the general trend in the field to overly concentrate on the *on/off* ratio of the devices, which have now reached extraordinary levels. It will actually be shown in §6.1 that this ratio is in reality one of the least important memory characteristics. Alternatively it could be that research has been conducted in this area, but possibly does not compare favourably with existing memory technologies.

A summary of the extremes reported for the different characteristics is included in Table 2.2, with the data being limited only to devices containing charge trapping nanoclusters or nanoparticles.

Table 2.2 Summary of reported device characteristics.

Characteristic	Minimum Reported	Maximum Reported
On/off ratio	10. [13, 92-93]	10^9. [86]
Retention time	> 3hours. [85]	Several weeks. [83-84]
Memory cycles	~50. [92-93, 95]	> 1 million. [83-84]

Of these characteristics the *on/off* ratio actually raises many questions regarding the working mechanisms of the PMDs. With ratios as high as 10^9 there are many reported devices which have *on* state currents in the microampere range, and in some cases even milliamperes. When considering that these are organic based materials with thicknesses of generally less than 100 nm and lateral dimensions of a few millimetres this results in incredibly high current densities.

As discussed previously, Scott [3] argued that any new technology must be able to compete with cutting edge memory devices in terms of; rated memory cycles, power consumption, retention time and price in order to be considered as a successor to any of the currently available memories, characteristics that so far PMDs fail to match in one or more areas. PMDs also have to offer performance which is at least equal to the foreseeable advances that are likely to be made by the established memory technologies in order to make it economically viable to switch to a new technology. While it is unclear whether PMDs will compete directly with existing memory technologies, or find their own niche market where price becomes a driving factor and performance requirements are not so strict, what is certain is that much work still needs to be done to improve performance.

Another area that has so far received little attention is demonstrating that arrays of memory cells are capable of storing useful amounts of data. All published work to date has been concerned with investigating single memory cells, usually via probe stations taking current-voltage measurements. To have a viable memory chip data needs to be able to be accessed in parallel, with all *read*, *write* and *erase* steps being performed directly under computer control. To achieve this circuitry has to be demonstrated that has the ability to interface between the PMD and a computer and be able to decode the state of many memory cells simultaneously.

Failures of devices have received no attention in published work, which can put doubt on any results obtained. For instance, many research groups publish *on* state currents on the order of tens to hundreds of microamperes. In devices that have dimensions of only a few millimetres squared and thicknesses of <100 nm, this leads to current densities, and electric fields in excess of the published breakdown strengths of many of the polymer materials used. In any device operating under these conditions there is doubt as to whether the device is actually suffering some form of electrical breakdown, rather than truly reversible electrical bistability.

In summary there are several areas of missing, or ambiguous data concerning PMDs that will each be investigated throughout the course of this research:

- Investigate the switching mechanisms in PMDs by scrutinising the proposed working mechanisms
- Conducting thorough investigations into the roles of the individual components which constitute a PMD to clarify the mechanisms responsible for the change in conductivity

- Performance related characteristics need to be studied, and in many cases improved.
- Degradation and failure mechanisms of devices will be investigated to better understand both the performance and the working mechanisms of PMDs.
- Design circuitry capable of interfacing with arrays of PMDs

One area where there is a surprising lack of knowledge is the electrical characteristics of polymer materials themselves. In the gold nanoparticle PMDs studied by Ouyang *et al.* [9] the bulk of the material in the device is polystyrene, but even basic electrical properties such as dielectric breakdown strength are unknown for the ultrathin polystyrene layers used. Previous investigations have been conducted, however, film thickness ranged from several hundred nanometres up to several micrometres and were primarily concerned with conduction mechanisms [106-107] and dielectric properties [108-109] As such a full investigation into the electrical properties of thin film polystyrene will be carried out, with dielectric breakdown strength as both a function of film thickness and anneal temperature investigated. The types and levels of trapped charges in polystyrene will also be investigated, with the data providing valuable evidence regarding the switching mechanisms in PMDs.

CHAPTER 3

Background Information to Insulator Carrier Transport Mechanisms and Scanning Probe Microscopy

Throughout this investigation there are several fundamental concepts and experimental techniques that are used on a regular basis, which form an integral part of many of the experiments that have been conducted. The first fundamental concept is the mechanism of carrier transport that may be applicable to the various materials used during the course of the investigation. This includes the conduction through both the organic and inorganic insulators, gold nanoparticles and admixture materials. Additionally experimental techniques based on scanning probe microscopy (SPM) are extensively used in many of the following chapters. Due to the prominence of conduction mechanisms and SPM techniques background information to the two will be introduced in this chapter. Other, more specialised experimental techniques will then be introduced in the chapters to which they apply.

3.1. Carrier Transport Mechanisms in Insulating Materials

An ideal insulating material is by definition "a body or substance that entirely or to a great degree prevents the passage of electricity … between contiguous bodies" [110] and in an ideal insulator the conductance is assumed to be zero. For real insulators however, this is not the case and under high electric fields or elevated temperatures conduction can occur. This is especially true of the thin insulating materials which are commonplace in the devices under study in this investigation.

The basic conduction processes that can take place are summarised in Table 3.1

Table 3.1 Summary of conduction processes in insulators [111].

Process	Full expression	Temperature dependence	Voltage dependence
Schottky emission	$J = A^{*}T^{2}\, exp\left[\frac{-e\left(\phi_B - \sqrt{e(V/d)/4\pi\varepsilon_i}\right)}{kT}\right]$ **Equation 3.1**	$\ln\left(\frac{J}{T^2}\right) \sim \frac{2\beta}{T}$	$\ln(J) \sim 2\beta V^{1/2}$

Poole-Frenkel emission	$J \sim \frac{V}{d}\ exp\left[\frac{-e\left(\phi_B - \sqrt{e(V/d)/\pi\varepsilon_i}\right)}{kT}\right]$ **Equation 3.2**	$\ln(J) \sim \frac{\beta}{T}$	$\ln\left(\frac{J}{V}\right) \sim \beta V^{1/2}$
Direct tunneling	$J \sim V\ exp\left[\frac{-2d\sqrt{2m^*\phi_B}}{\hbar}\right]$ **Equation 3.3**	none	$J \sim V$
Fowler-Nordheim tunneling	$J \sim \left(\frac{V}{d}\right)^2\ exp\left[\frac{-4d\phi_B^{3/2}\sqrt{2m^*}}{3e\hbar V/d}\right]$ **Equation 3.4**	none	$\ln\left(\frac{J}{V^2}\right) \sim \frac{\alpha}{V}$
Space charge limited	$J = \frac{9}{8}\frac{\varepsilon_i \mu V^2}{d^3}$ **Equation 3.5**	none	$J \sim V^2$
Ohmic	$J \sim \frac{V}{d}\ exp\left[\frac{-\Delta E_{ae}}{kT}\right]$ **Equation 3.6**	$\ln(J) \sim \frac{\gamma}{T}$	$J \sim V$
Ionic	$J \sim \frac{V}{dT}\ exp\left[\frac{-\Delta E_{ai}}{kT}\right]$ **Equation 3.7**	$\ln(JT) \sim \frac{\delta}{T}$	$J \sim V$

Where J is the current density, A^* is the Richardson constant, ϕ_B is the barrier height, ε_i the insulator permittivity, d is the insulator thickness, m^* is the effective mass, μ the charge carrier mobility and E_{ae} and E_{ai} the activation energy of electrons and ions respectively. Device dependent constants are α, β, γ and δ.

Schottky emission is a contact limited process where current is limited by thermionic emission over the metal-insulator barrier. Poole-Frenkel emission is a bulk limited process with field-enhanced thermal excitation of trapped electrons in the insulator. For thin insulating layers the tunneling mechanisms can become dominant, with direct tunneling being through a square barrier, while Fowler-Nordheim tunneling is through a triangular barrier, as could be the case at higher electric fields.

Space charge limited conduction (SCLC) is as a result of carriers being injected into the insulator from the electrodes when there is no compensating charge present in the insulator. Ohmic conduction results from thermally excited electrons at higher temperatures, while ionic conduction is as a result of ionic impurities moving through the insulator under high electric fields. This later mechanism would be expected to decay with time as the charges

move to the metal-insulator interfaces but are unable to be injected or extracted through the interface.

In polymer materials with film thicknesses in the range nanometres to micrometres conduction usually takes the form of Schottky or Poole-Frenkel emission [106-107, 112-113], though differentiation between the two is sometimes hampered due to the similarities in their resultant *I-V* characteristics.

3.2. Scanning Probe Microscopy

Scanning probe microscopy is the generic name for the family of scanning techniques that are based on bringing a probe (or, more usually a tip in the case of scanning tunneling microscopy) in close proximity to a surface and measuring the interactions between the probe and the surface. Due to the small dimensions at the apex of the probe (typically on the order of tens of nanometres radius of curvature) SPM techniques offer the possibility of atomic scale imaging of sample surfaces. The origins of SPM date back to the invention of the Scanning Tunneling Microscope by Binnig and Rohrer in 1981 and their subsequent publications [114-115], with the Atomic Force Microscope being demonstrated in 1986 [116]. Subsequent improvements have also lead to the development of a large range of modes, each measuring a specific interaction between the probe and substrate. By using these modes it is not only possible to investigate topographical features, but also other material properties such as friction, magnetism and electrostatic forces among many others. Unless explicitly stated, all the SPM measurements during this research were carried out on a Park Systems XE-100 SPM.

3.2.1. Scanning Tunneling Microscopy (STM)

Scanning tunneling microscopy is based on the principal of quantum tunneling between a conducting tip and the conducting or semiconducting substrate under investigation. A schematic of the operation of an STM is shown in Figure 3.1. When the tip is brought into close proximity with the surface (with separations on the order of a few angstroms) then a measurable current flows between the two due to the finite probability of electrons tunneling through the insulating barrier between the tip and sample. Two possible modes of operation can be used, namely, constant height and constant current. In constant height, the tip is kept at a constant height above the substrate as it is scanned, with the tunneling current varying, thereby allowing a topography image to be constructed. In constant current mode a set

tunneling current is maintained between the tip and sample by adjusting the tip-sample distance. The topography image is then constructed directly from the height of the tip.

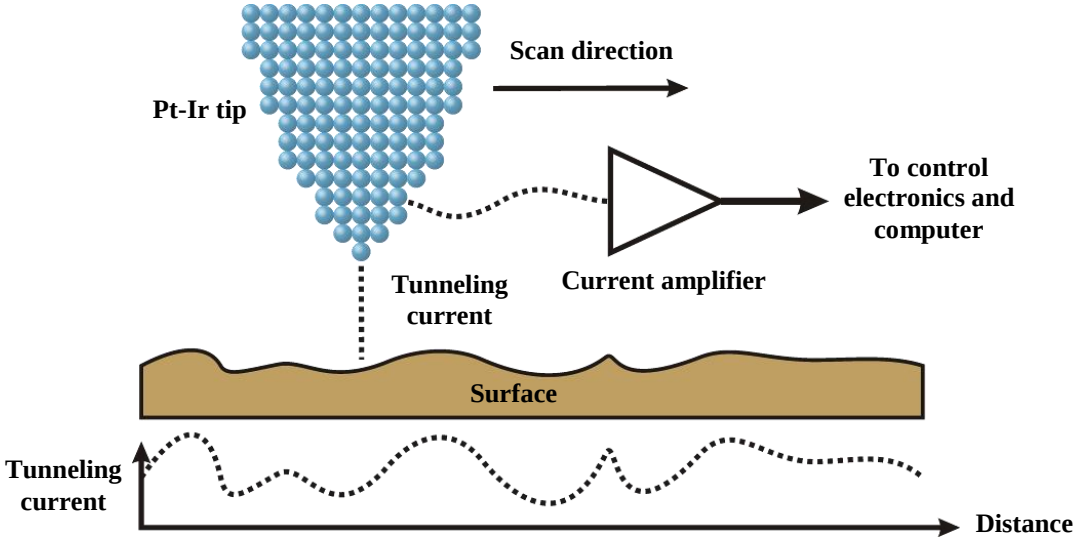


Figure 3.1 Schematic of an STM system in constant height mode.

In this investigation a tip made from platinum-iridium wire was used in all cases, due to its resistance to oxidation in air. The tips were fabricated via mechanical methods by severing the wire with cutters, while applying tension with pliers. Another common method for fabricating STM tips involves the electrochemical etching of tungsten wire. This method wasn't used here primarily due to the added complexity of fabrication and the tendency of the produced tips to be slightly blunt. Etching tips does however result in reproducible fabrication of tips, while mechanical cutting is dependent on practice and user skill.

3.2.2. Atomic Force Microscopy (AFM)

In atomic force microscopy the conducting tip is replaced by a probe mounted on a flexible cantilever (shown in Figure 3.2(a)). The forces that are present between the probe and the sample then form the basis of the measurement system for constructing the surface topography of the sample. Two scanning modes are routinely used and are available on the XE-100 system; contact (static) mode and non-contact (dynamic) mode. In contact mode the tip is in physical contact with the surface, operating in the region where interatomic forces repel the tip away from the sample (Figure 3.2(b)). In this way the tip follows the surface features, while feedback mechanisms maintain a constant force between the tip and sample. In non-contact mode the tip is positioned above the sample in the region where attractive forces dominate (Figure 3.2(b)). A small alternating signal is then applied to the cantilever

forcing it to oscillate. The interactions between the tip and sample cause variations in the amplitude and phase of the oscillations, which are used to construct the surface topography image.

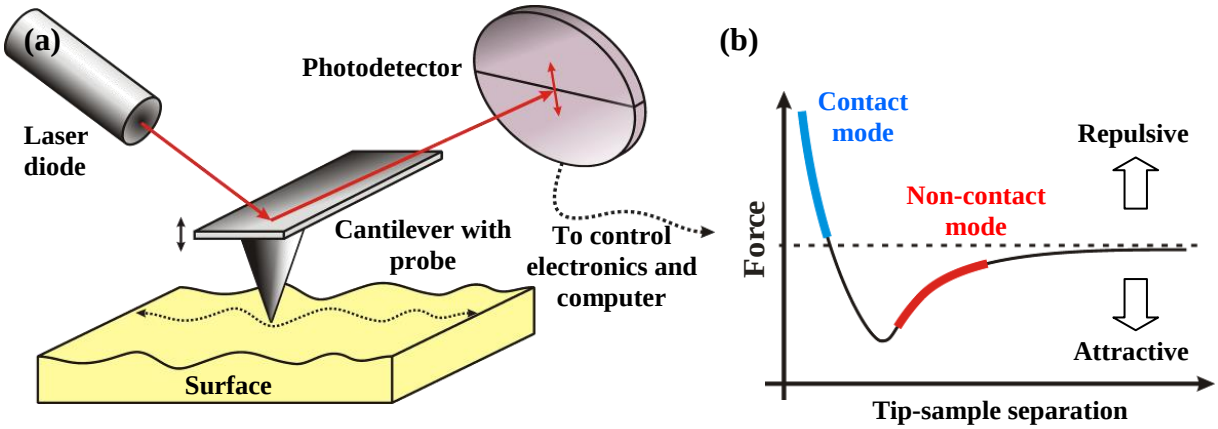


Figure 3.2(a) Schematic of an AFM operating in contact mode. (b) Interatomic forces vs. distance graph showing regions where different AFM modes operate.

There are also many additional modes that are available by using probes with different material properties. The main one of these modes that will be used extensively in Chapter 5 is electrostatic force microscopy (EFM). In this mode a voltage is applied to a conductive probe to sense the electrostatic forces between the probe and the sample, as illustrated in Figure 3.3.

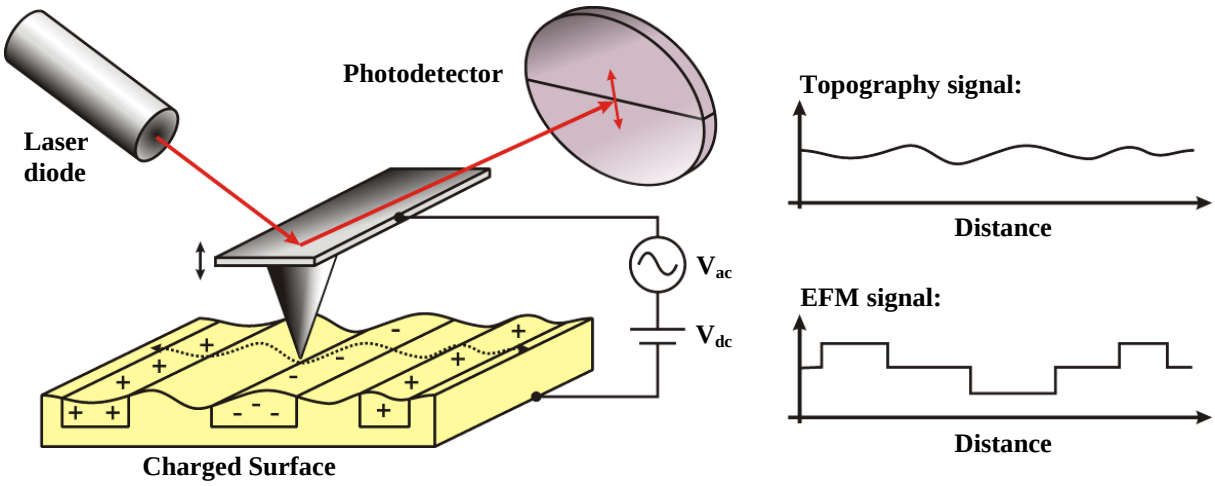


Figure 3.3 EFM measurement principal.

With this technique locally charged areas of a substrate or sample can be detected and measured. This mode will be extensively utilised in experiments concerned with the charging properties of gold nanoparticles and nanoparticle containing films.

CHAPTER 4

Optimisation of Polystyrene Deposition and Electrical Characterisation of Polystyrene Thin Films

As discussed in §2.3 despite polystyrene being used in several polymer memory devices to date, there is still a large knowledge gap concerning the electronic properties of polystyrene. Until these properties are fully investigated it is not possible to rule out the possibility that the polystyrene itself is playing a role in the memory mechanism.

Until recently traditional insulating polymers had never been considered for microelectronic applications, hence the bulk of the information available pertains to mechanical and chemical properties, with electrical information limited to properties relevant to bulk material insulating applications. The first steps towards understanding how PMDs function is to have reliable data for the electrical properties of the polystyrene used as the insulating matrix in the devices. This chapter aims to address the following:

- The justification for the choice of polystyrene as the polymer insulator.
- Optimisation of the polystyrene layer to achieve the optimum electrical performance.
- Testing of various structures to calculate the electronic data relevant to PMDs, and the associated theory related to the tests.

4.1. Choice of Polystyrene

One of the main driving factors in the use of polystyrene as the main polymer constituent of the PMDs is the fact that the majority of the most recent metal nanoparticle devices utilise polystyrene as an insulating matrix [9-10, 16]. In order to study devices as alike as possible to these, polystyrene needs to be used so as to not introduce extra factors into the electrical characteristics.

However, the choice of polystyrene (due to its good balance of characteristics when compared with other polymers) is actually beneficial for several other reasons as outlined below:

- Moisture absorption <0.1% [117] - Due to the adverse effects that moisture absorption can have on the electrical characteristics of devices a low value here is

highly desirable. Polystyrene has one of the lowest water absorptions among commercially available polymers.

- Dielectric strength: 0.2 – 0.8 $MV \cdot cm^{-1}$ [117].
- Dielectric Constant: 2.4 – 2.7 [117].
- Large choice of solvents [118]. Importantly, the main solvents used (dichlorobenzene, chloroform and toluene) are also solvents of the other PMD constituents such as the gold nanoparticles, hence homogeneous admixtures can easily be achieved.
- Readily commercially available.

However, the electrical properties mentioned above are for the bulk material. In regard to thin films (<200 nm) there was no available literature when this work was undertaken. In §4.3 there follows a discussion concerning the applicability of the bulk values when thin films are used.

4.2. Spin-Coater Calibration and Polymer Layer Optimisation

There are a number of techniques by which polymer thin films can be deposited, for example; dip-coating, spray coating, spin-coating and chemical vapour deposition (CVD) methods. In this work the spin-coating technique was employed for the fabrication of PMDs. As the polymer admixture layer is fabricated solely by spin-coating, this has the greatest potential to influence device characteristics if the process is not optimised correctly and under control at all times.

To this end the main parameters that were likely to affect the quality and thickness of the final spin-coated layer were identified. The two main parameters in spin-coating are:

- Polymer solution concentration.
- Final spin-coating speed.

However, the following were also identified as possibly having minor effects:

- Spread speed. (An initial low speed spin which distributes the solution across the substrate).

- Static or dynamic spin-coating. (Static:- the solution is dispensed before the substrate starts spinning. Dynamic:- the solution is dispensed once the substrate has begun spinning).
- Amount of polymer solution dispensed.
- Acceleration up to final coating speed.
- Substrate material and size.
- Substrate surface.

Experiments were conducted to assess the influence of each of the parameters using polystyrene dissolved in dichlorobenzene as the polymer solution. For the majority of experiments 25 mm^2 p-type silicon was used for the substrate material. The exception to this was during experiments requiring a change to the substrate size, or material, where 10 mm^2 p-type silicon and 25 mm^2 glass substrates were used respectively. In all cases five depositions were made and an average polymer thickness obtained. Film thicknesses were measured using a Rudolf Research Auto Ellipsometer. At the same time, refractive index data was also collected, as this can give an indication of the quality of the polymer layer, due to the way it can be related to the dielectric constant. The refractive index of a material, *n*, can be defined according to the equation:

$$n = \sqrt{\mu_r \varepsilon_r} \qquad \textbf{Equation 4.1}$$

Where μ_r and ε_r are the relative permeability and permittivity (dielectric constant) respectively. For non-magnetic materials μ_r is ~1, hence Equation 4.1 reduces to:

$$n^2 = \varepsilon_r \qquad \textbf{Equation 4.2}$$

Thus a direct measure of the dielectric constant can be made by measuring the refractive index.

To investigate the effect of varying the concentration of the polymer solution versus final spin speed, spin speeds were varied from 2,000 – 10,000 rpm, while concentrations of 15 – 55 mg of PS per millilitre of solvent were used, increasing in 10 mg increments. Other parameters were kept constant at 500 rpm spread speed and an acceleration of approximately 2000 rpm per second. These results are plotted in Figure 4.1, with the inset showing the variation in the refractive index of the PS for all measurements taken.

As would be expected, both higher concentrations of PS solution and lower final spin speed result in thicker deposited films. From the refractive index data it can be seen that all

the concentrations from 25 mg·ml^{-1} and above match with the theoretical refractive index of ~1.6 [117] (and hence from Equation 4.2 also match with the theoretical dielectric constant). This means that solution concentrations of 25 mg·ml^{-1} and above will likely result in films with optimum material properties.

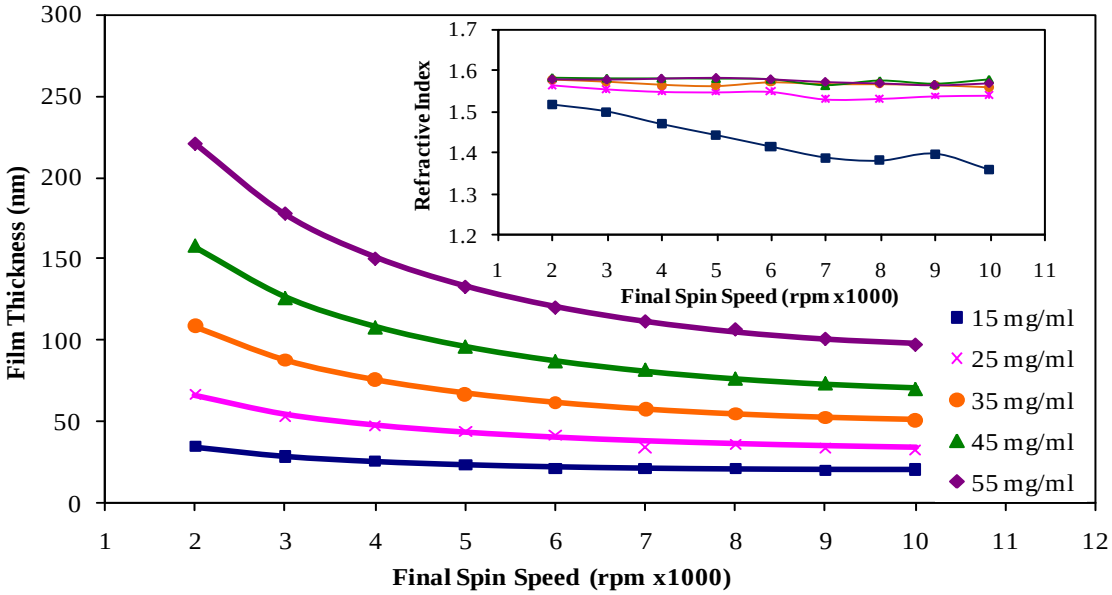


Figure 4.1 Polymer film thickness vs final spin speed. (Inset: Refractive index vs final spin speed).

Table 4.1 summarises the results of experiments into the remaining factors that were identified as likely to have an effect on the film thickness.

Table 4.1 Summary of spin-coater parameter effects.

Parameter	Effect
Spread speed	Higher spread speeds result in thicker films. Each increase of 100 rpm increases film thickness by ~1.6% for spread speeds from 200 – 1000 rpm. (See Appendix E for additional data).
Static or dynamic spinning	Films are ~10% thinner when dynamic mode is used. (See Appendix E for additional data).
Amount of solution dispensed	No effect, provided sufficient solution is dispensed to fully coat the substrate.
Substrate material and size. Substrate surface. Acceleration rate of spinner.	No effect, provided the solution has a good wettability of the substrate.

Out of these parameters only the spread speed and static/dynamic spinning had a measurable difference on the final film thickness.

From these calibration experiments polystyrene films ranging in thickness from 35 nm to over 200 nm can be deposited, while still ensuring that good quality electrical characteristics are retained.

In parallel with the spin-coater calibrations, efforts were also made to improve and optimise the quality of the deposited polystyrene films. Initial films showed visual evidence of defects in the form of both particulates and pinholes which will lead to electrical weak points in devices where failure is likely to occur. Films were investigated both at the macroscopic scale under an optical microscope and at the microscopic scale via AFM. At both scales a large number of defects are evident, as illustrated by Figure 4.2(a) and (b).

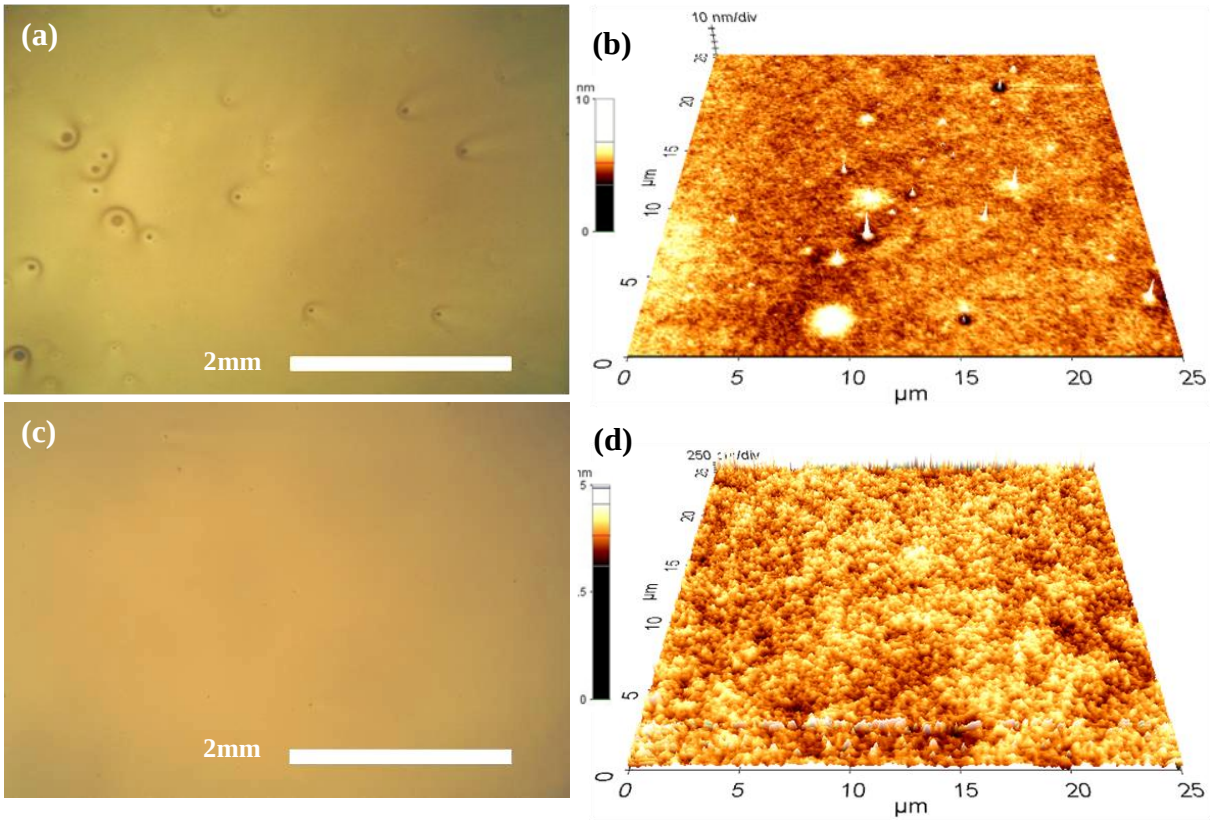


Figure 4.2 Defects in polystyrene films. (a) Optical image before filtration. (b) AFM image before filtration. (c) Optical image after filtration. (d) AFM image after filtration.

From analysis of Figure 4.2(b) approximately 30 defects are easily identifiable (i.e. >500 nm in size). Assuming similar defect densities are present across the substrate this would lead to defect densities in the order of ~50,000 mm^{-2}. To minimise defect densities all polymer solutions were subsequently filtered through 0.7 μm pore size chemically resilient filters to remove any larger particulates. The reduction in defects can clearly be seen in Figure 4.2(c) and (d).

4.3. MIM Current – Voltage Characteristics

To study the basic electrical characteristics of polystyrene, such as dielectric breakdown strength and conduction mechanisms, MIM structures were fabricated and tested with a computer controlled picoammeter.

4.3.1. Dielectric Strength

Dielectric strength of polymer materials can be dependent on several factors, such as molecular weight and polymer grade. As such the values found in literature can have a large amount of uncertainty and cannot be relied upon, hence a thorough investigation was undertaken to determine the exact dielectric strength of the polystyrene used, rather than relying on published data. The effect of two variables on the dielectric strength has been investigated; namely film thickness and anneal temperature. The justifications for investigating these two parameters are given in the following paragraph.

It has previously been reported that thin films of PTFE (<500 nm) show significantly higher dielectric strengths than the bulk material. It is reasonable to assume that PS may also behave similarly. Processing factors, such as low temperature anneals at temperatures up to approximately the glass transition temperature, but below the melting temperature (T_g = 100°C, T_m = 240°C for PS [117, 119]) could also result in relaxation of the films affecting the dielectric strength.

At this point it is also prudent to include a brief note about the glass transition temperature of the experimental films. The T_g value has been shown to have some dependence on both the molecular weight of the polymer and the film thickness [120-121]. For the film thicknesses studied here (>45 nm) these effects combine to a maximum likely deviation away from the bulk T_g of approximately 5 °C. As it is possible to find at least this much discrepancy in the published values of T_g from different sources [122] these effects will be neglected, and a T_g value of 100 °C assumed for all samples.

In all cases the breakdown point of the polymer films is defined as the point at which the devices became short circuited as illustrated by the *I-V* curve shown in Figure 4.3.

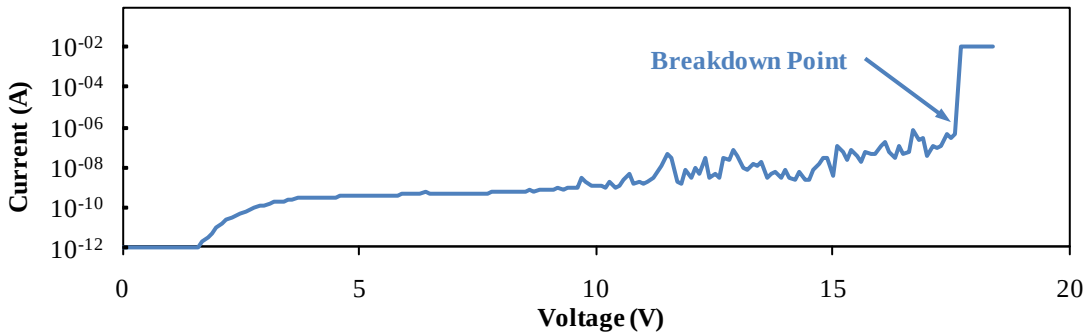


Figure 4.3 *I-V* characteristics of polystyrene MIM structure with aluminium electrodes, showing the breakdown point.

The first set of experiments were conducted on films with a range of thicknesses from 45 nm to 120 nm in steps of 15 nm, with no anneal step performed on the samples. The second set of experiments to investigate anneal effect were conducted on films with a constant 45nm thickness. Anneals were performed for 30 minutes in atmospheric conditions at temperatures between 30 °C and 120 °C with 15 °C intervals. All the anneals were carried out before the evaporation of the top aluminium contact to ensure that there was no possibility of any interaction between a softening polystyrene film and the top electrode.

The results of the thickness dependence of the dielectric strength are shown in Figure 4.4(a), while Figure 4.4(b) shows the dependence on anneal temperature.

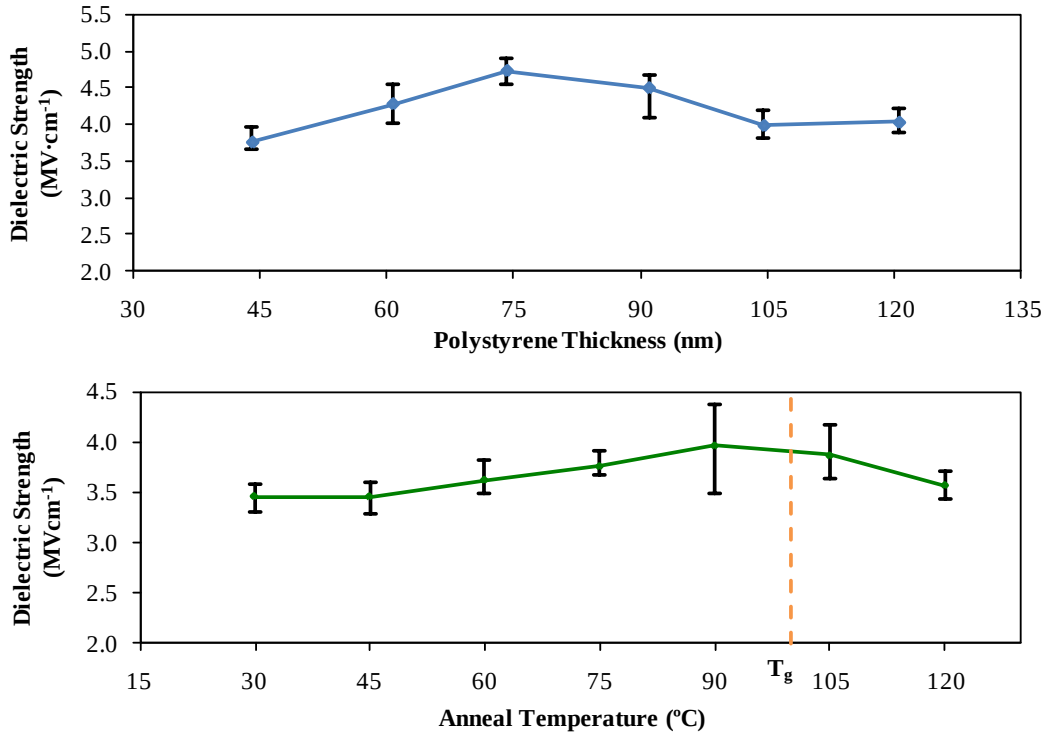


Figure 4.4 Dielectric Strength as a function of (a) Film thickness. (b) Anneal temperature. Error bars represent the range of values for all data collected.

The initial outcome of the experiments to note, is the high dielectric strength which is approximately an order of magnitude higher, compared to the bulk polystyrene value. As mentioned previously this phenomenon has been reported in other polymer materials [123] and can be attributed to a combination of factors that change for thin films, including; film morphology, material structure, charge trapping and de-trapping characteristics, all leading to a change in the breakdown mechanism of the films away from an electromechanical breakdown mechanism that dominates in thick films.

From Figure 4.4(a) a maximum dielectric strength of 4.7 $MV \cdot cm^{-1}$ was found at a film thickness of 75 nm. As well as the dielectric strength starting to decrease with increasing film thickness, there is also a trend for the strength to start decreasing for films thinner than 75 nm. The exact origins of this decrease are outside the scope of this investigation, but could be related to the fact that the refractive index also starts to decrease for these films (see inset of Figure 4.1) which indicates that the quality of these ultrathin films also starts to decrease.

The dielectric strength as a function of the anneal temperature shows an increasing trend to the point where the glass transition temperature is reached. Further increases in anneal temperature then lead to a gradual decrease in the dielectric strength. At temperatures below T_g the polymer is in its glassy state, where bonds between polymer chains are intact and movement between chains is not possible. As the temperature approaches T_g the bonds weaken and allow the polymer chains to move, resulting in a rubbery state above T_g. This movement of polymer chains and removal of any internal stresses due to relaxation effects could be responsible for the decrease in dielectric strength above T_g, as it is possible that pinholes and weak areas could actually be introduced into the films as it becomes more mobile. However, the increase in dielectric strength at anneal temperatures below T_g cannot be explained as readily as polymer chains should be immobile below this value. Closer inspection of the films before and after annealing revealed that the film thickness decreased marginally for higher temperature anneals, as shown in Figure 4.5.

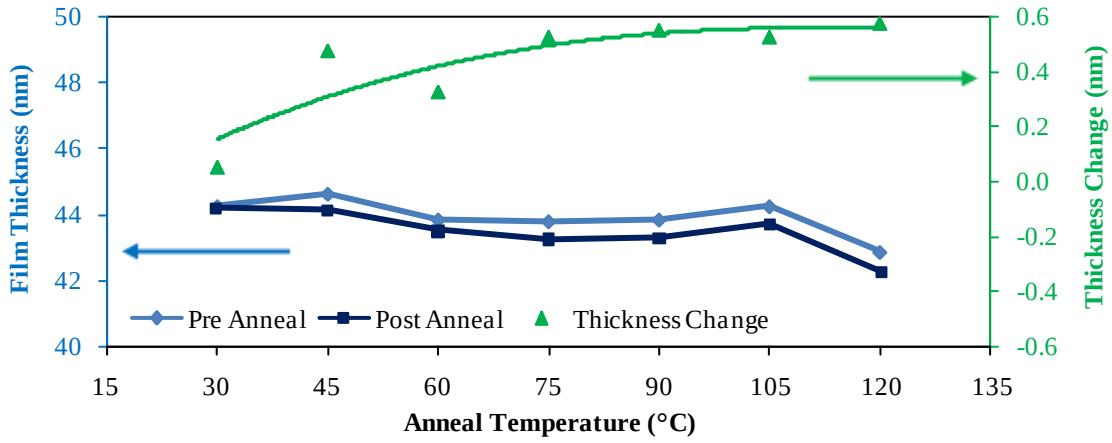


Figure 4.5 Effect of anneal temperature on film thickness.

At higher anneal temperatures the effect results in an approximately 1% reduction in film thickness. This decrease is likely due to residual solvent from the fabrication process being driven out of the polystyrene. As fewer impurities are present in the film, this could result in the increase in dielectric strength between room temperature and T_g.

4.3.2. Conduction Mechanisms in Polystyrene

As discussed in §3.1 there are several conduction mechanisms that are possible in insulating materials. It is also possible that a particular conduction mechanism may not be exclusively responsible, with a combination of mechanisms, or a change in mechanism possible dependent upon the temperature and applied voltage.

A knowledge of the particular conduction mechanisms that are present in polystyrene is important, as it can give an insight into possible mechanisms that are responsible for the conductivity change in PMDs. With the polystyrene thicknesses concerned and at room temperature, the likely conduction mechanisms are either Poole-Frenkel emission, or Schottky emission. From Table 3.1 it can be seen that these two mechanisms both have similar voltage and temperature dependences, resulting in difficulty distinguishing between the two. However, both mechanisms can be expressed in simplified forms [107, 124] with Schottky emission taking the form:

$$J = J_0 exp\left(\beta V^{1/2}\right) \qquad \textbf{Equation 4.3}$$

While Poole-Frenkel takes the form:

$$J/V = J_0 exp\left(\beta V^{1/2}\right) \qquad \textbf{Equation 4.4}$$

Where from Equation 3.1 and Equation 3.2:

$$\beta_{PF} = 2\beta_S = \frac{1}{kT}\left(\frac{e^3}{\pi\varepsilon_o\varepsilon_r d}\right)^{1/2} \qquad \textbf{Equation 4.5}$$

As can be seen, the β coefficient is twice as large in Poole-Frenkel emission, compared to Schottky emission, suggesting the two mechanisms can be distinguished by studying *I-V* data. The measured *I-V* characteristics of the polystyrene MIM devices can be plotted as $J\ vs. V^{1/2}$ and $J/V\ vs. V^{1/2}$ to enable the experimental β value to be calculated and compared with theoretical values. Typical $J\ vs. V^{1/2}$ and $J/V\ vs. V^{1/2}$ plots are shown in Figure 4.6(a) and (c) respectively, with the β values calculated from the linear portion of the graphs. β values were calculated from PS MIM diodes measured at ~300 K with a range of insulator thicknesses, chosen to cover the most common insulator dimensions used throughout this investigation. Comparisons of the experimental β values are shown in Figure 4.6(b) and (d), along with the theoretical β_{PF} and β_S values.

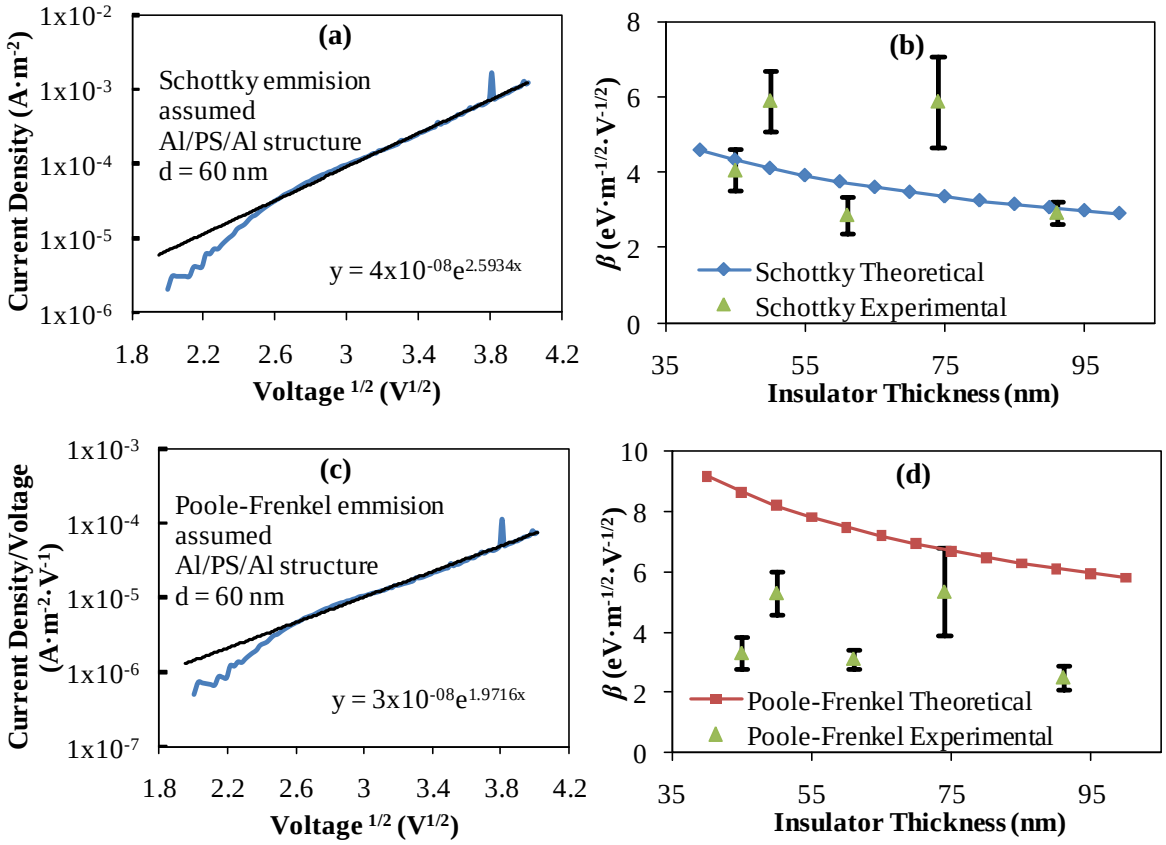


Figure 4.6(a) Typical *J vs* $V^{1/2}$ data for a PS MIM diode. (b) Theoretical and experimental *β* values assuming Schottky emission. (c) Typical *J/V vs* $V^{1/2}$ data for a PS MIM diode. (d) Theoretical and experimental *β* values assuming Poole-Frenkel emission (Error bars show the standard deviation of the data).

From the experimental values of β it is clear that there is a large amount of experimental spread in the data. In general the experimental values tend towards Schottky emission being the dominant conduction mechanism in polystyrene at room temperature. However, the data is not conclusive due to the large variation in experimental β values. To confirm the dominant mechanism another method to distinguish the two mechanisms is needed. As Poole-Frenkel emission is a bulk limited process, while Schottky emission is contact limited, this suggests that by changing the electrode material and hence the electrode work function, then with Schottky emission the *I-V* characteristics will show asymmetry if dissimilar electrodes are used. The metals chosen for the investigation (and their work functions in eV [125]) were aluminium(4.28), indium(4.12), copper(4.65) and chromium(4.5), with all top and bottom contact combinations fabricated. It was found that some of the contact combinations resulted in devices that were short-circuited and hence not viable. Devices with gold-gold and aluminium-gold contacts were also fabricated to investigate the effect of the higher work function of gold (5.1 eV), however these devices were short-circuited and no reliable data could be obtained. Table 4.2 summarises the metal combinations used and the viability of the structure.

Table 4.2. Viability of contact combinations in MIM devices.

		Top Contact			
		Aluminium	**Indium**	**Copper**	**Chromium**
Bottom Contact	**Aluminium**	Yes	Yes	Yes	No
	Indium	Yes	No	No	No
	Copper	Yes	Yes	Yes	No
	Chromium	Yes	Yes	Yes	No

The main unviable devices consisted of indium bottom contacts and chromium top contacts. The reasons for the shorted devices are unknown, but could be related to reactions taking place between some metals and the polystyrene layer. In the case of the chromium it could also be related to the high melting temperature of the metal, resulting in higher evaporation chamber temperatures which could damage the polymer layer. (See also §5.3). For similar metal electrodes the *I-V* characteristics were found to be symmetrical between the positive and negative voltage scans (Figure 4.7(a)), as would be expected for both conduction mechanisms. However, for the viable devices where different metal contacts were used

asymmetry was evident as shown in Figure 4.7(b) and (c). This confirms that the dominant conduction mechanism in polystyrene at room temperature is likely to be Schottky emission.

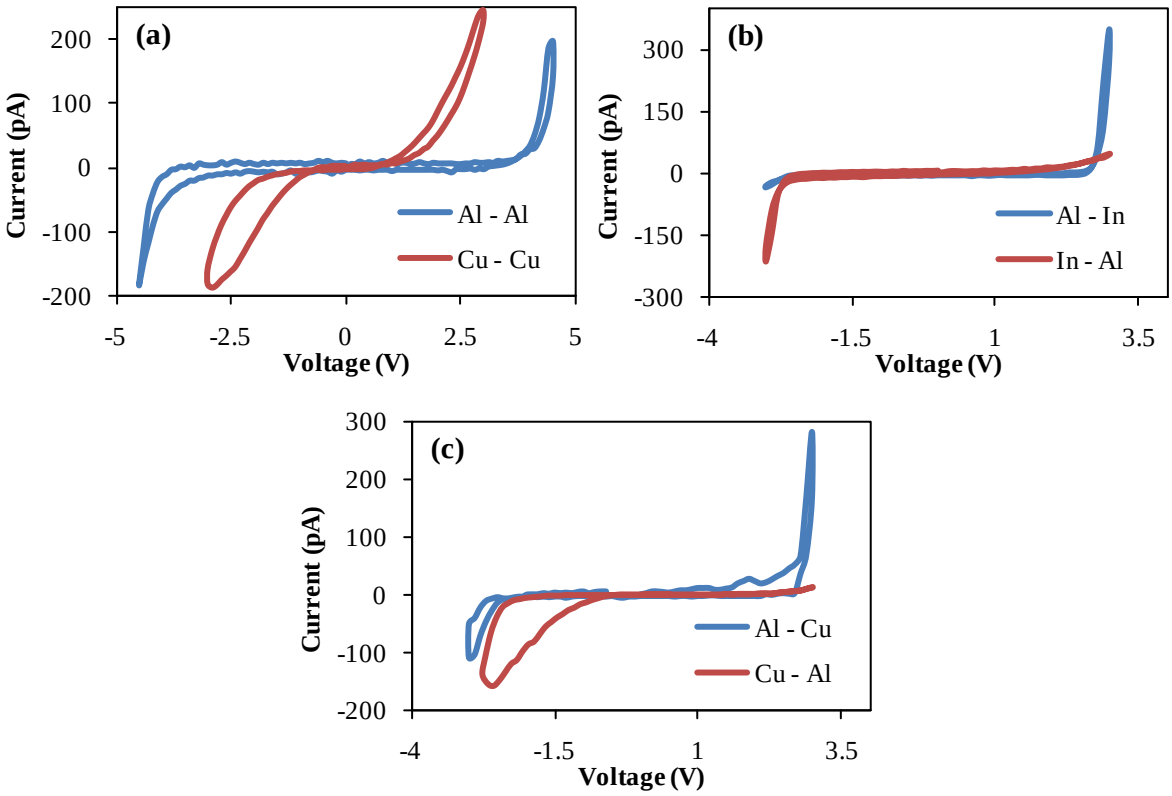


Figure 4.7 *I-V* characteristics of MIM diodes with differing electrode metals.

4.4. MIS Capacitance – Voltage Theory and Justification

One of the areas of uncertainty when using polymer materials is the role of impurities and trapped charges that may be present in the devices and the effect that these may have on the characteristics and working mechanisms of PMDs. When compared to traditional semiconductor materials, which routinely achieve purity levels as high as 99.999999999% [126], the polymers, chemicals and molecular materials used throughout this work rarely achieve purities above 99.9% and in some cases purity information is unavailable. As such, the role of impurities cannot be immediately eliminated, and experiments to determine the effects of impurities and the trapped charges that may be present in devices were designed and implemented.

In conventional semiconductor devices impurity and trapped charge information concerning the insulating material in question (predominantly SiO_2) can be obtained by studying *C-V* curves of MIS capacitors [111]. In particular information can be extracted relating to the following:

- Interface trapped charge (Q_{it}).
- Fixed insulator charge (Q_f).
- Insulator trapped charge (Q_{inst}).
- Mobile ionic charge (Q_m).

The trapped charge values extracted from the experimental results also depend on the device geometry (as they give the total charge present in the device). As the exact geometry of all devices is known, it is then a trivial matter to calculate the number of charges per unit area from the following.

$$D = \frac{Q}{eA} \qquad \textbf{Equation 4.6}$$

Where A is the device area and e is the elementary charge. This gives device independent results relating only to the polymer insulator. These charge densities are defined as D_{it}, D_f, D_{inst} and D_m respectively for the four charge types.

The relative positions in which these types of charge can be found in the cross-sectional structure of the MIS capacitor are shown in Figure 4.8.

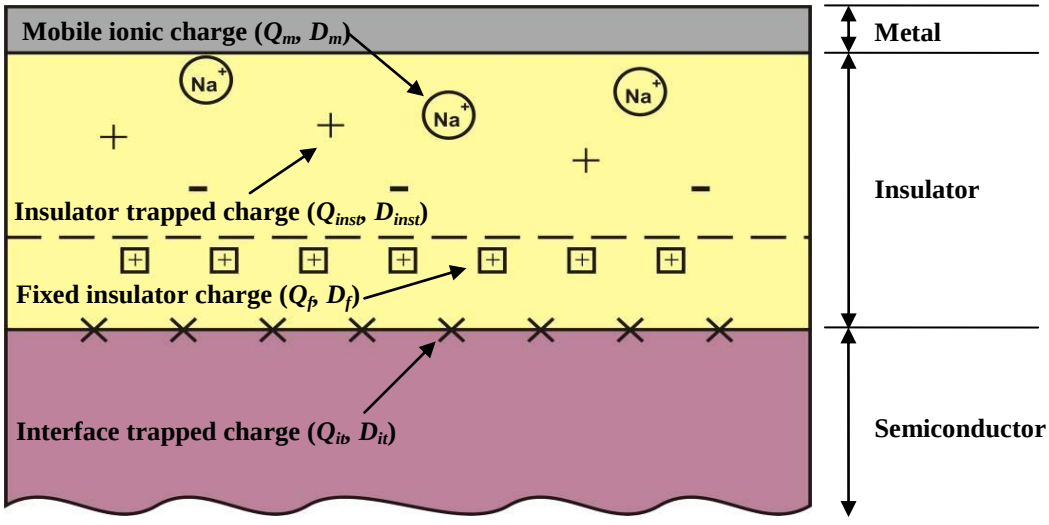


Figure 4.8 Metal-insulator-semiconductor capacitor structure and location of charges [111].

Either p-type or n-type silicon can be used as the substrate material for the capacitors, however, due to the different majority carriers between the two, the theory of operation differs. All of the following theory relates to the use of a p-type silicon substrate as the basis

for the MIS capacitors, though if n-type were used the same effects would be seen, but at opposite voltage polarities.

To understand the theory behind how an MIS capacitor works and how the structure can be used to extract insulator charge information, firstly consider a conventional parallel plate capacitor. Here, a dielectric material is sandwiched between two metal electrodes, with the capacitance being a function of the area of the electrodes, A, the distance between electrodes, d and the relative permittivity of the dielectric, ε_r, according to the equation:

$$C = \frac{\varepsilon_r \varepsilon_0 A}{d} \qquad \textbf{Equation 4.7}$$

However, in an MIS capacitor, the capacitance is also a function of the frequency and the voltage applied across the capacitor. This gives rise to three distinct regions in the *C-V* curve, namely accumulation, depletion and inversion, as shown in Figure 4.9.

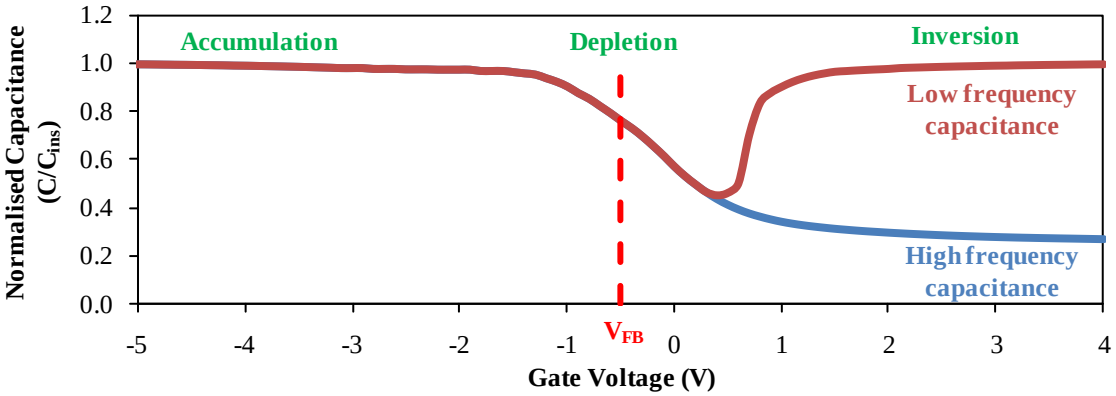


Figure 4.9 Typical high and low frequency MIS C-V Curves with p-type substrate.

By considering the energy band structure of the MIS capacitor, the differences in behaviour in the three regions can be described, with Figure 4.10 showing the energy bands of an ideal device at flatband conditions where there is no band bending present in the semiconductor.

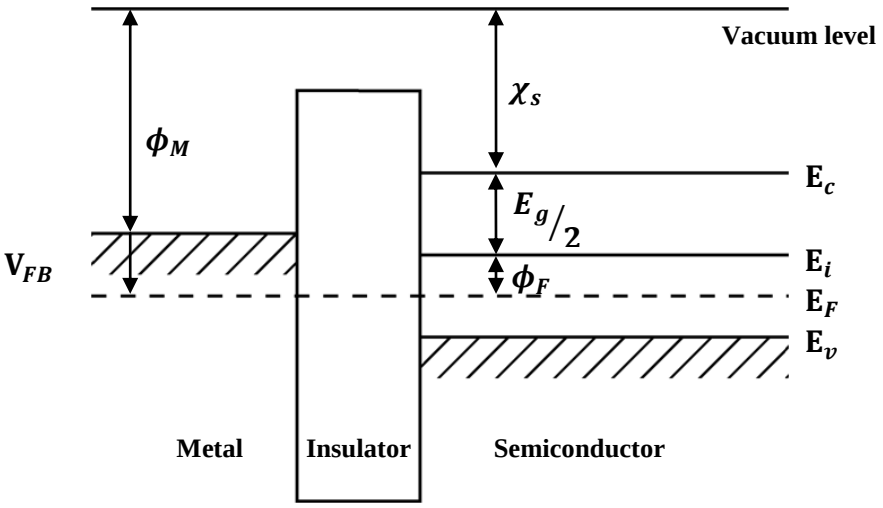


Figure 4.10 Metal-insulator-semiconductor capacitor energy band diagram.

In an ideal MIS capacitor with no trapped charges present, the voltage that has to be applied to reach flatband conditions is the flatband voltage (V_{FB}) and is equal to the work function difference between the metal and semiconductor, ϕ_{MS}. It then follows that:

$$\phi_{MS} = \phi_M - (\chi_s + {}^{E_g}/_2 + \phi_F) \qquad \textbf{Equation 4.8}$$

Where ϕ_F can easily be calculated from the well known semiconductor equation:

$$\phi_F \approx kT \ln\left(\frac{N_A}{n_i}\right) \qquad \textbf{Equation 4.9}$$

Where N_A is the doping concentration, and n_i is the intrinsic carrier concentration. At flatband voltage conditions the capacitance value is defined as the flatband capacitance.

4.4.1. Accumulation

When a negative voltage is applied to the gate of the MIS capacitor the energy bands bend upwards at the semiconductor surface, as shown in Figure 4.11. This leads to an accumulation of holes (the majority carriers for p-type silicon) and hence a positive charge appearing at the semiconductor surface. This positive charge is separated from the negative gate charge by the insulating material only, hence the resulting capacitance is simply the capacitance of the insulating layer, C_{ins} and can be calculated in the same way as a parallel plate capacitor from Equation 4.10, where t_{ins} is the thickness of the insulator.

$$C = C_{ins} = \frac{\varepsilon_{ins}\varepsilon_0 A}{t_{ins}} \qquad \textbf{Equation 4.10}$$

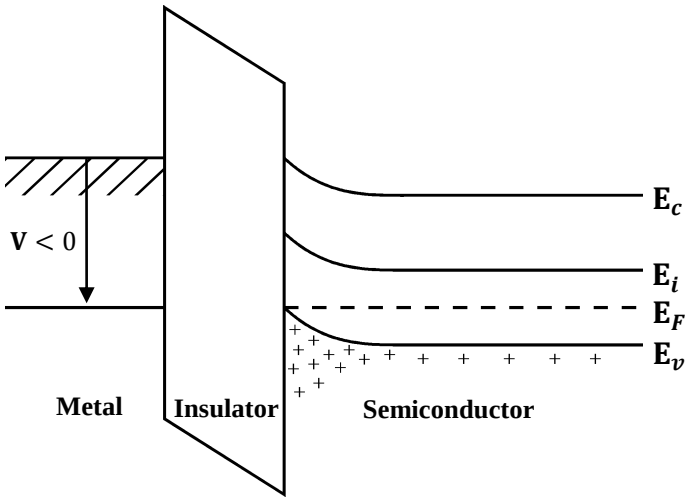


Figure 4.11 Accumulation region energy band diagram.

4.4.2. Depletion

When a moderate positive voltage is applied to the gate the holes at the semiconductor surface are repelled away from the insulating layer, resulting in a depletion region being formed, giving rise to the band structure in Figure 4.12.

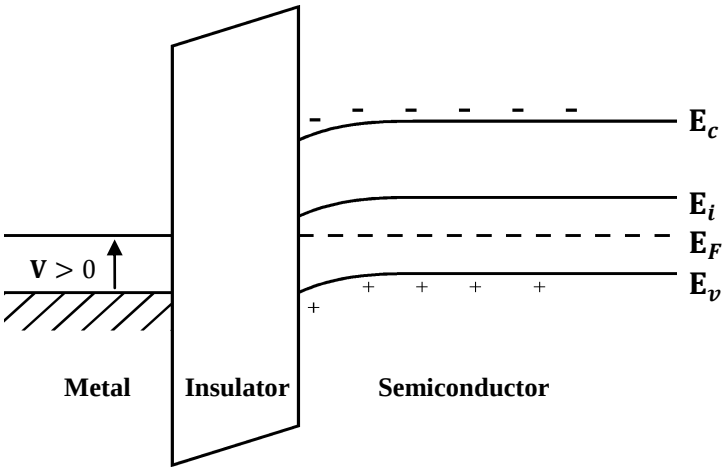


Figure 4.12 Depletion region energy band diagram.

In this region the depletion layer thickness is strongly dependent upon the applied voltage and so the total capacitance is a series combination of the insulator capacitance and the depletion layer capacitance, C_D as given by Equation 4.11:

$$C = \frac{C_{ins}\, C_D}{C_{ins} + C_D} \qquad \textbf{Equation 4.11}$$

Hence as the depletion layer increases in thickness the total capacitance reduces.

4.4.3. Inversion

If the gate voltage is further increased then the energy bands bend far enough for the semiconductor intrinsic level to bend below the Fermi level, inverting the surface of the semiconductor to form n-type silicon, as shown in the band structure in Figure 4.13.

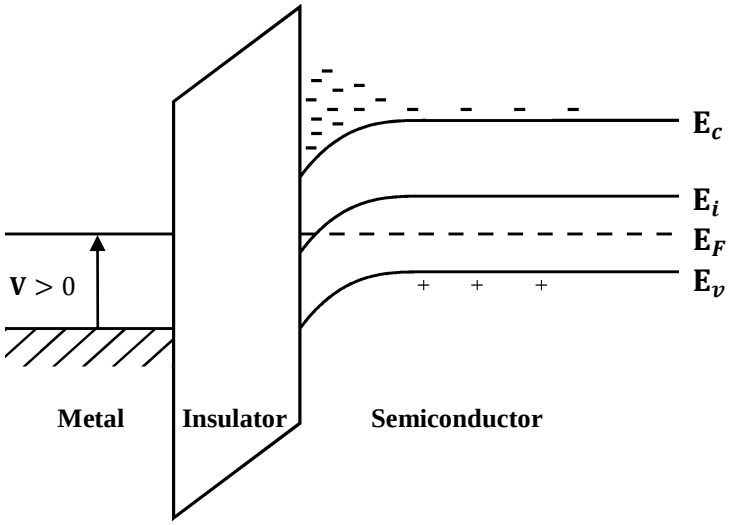


Figure 4.13 Inversion region energy band diagram.

The electrons that are now at the semiconductor surface are the minority carriers in p-type silicon, so have a slow generation rate and will respond differently depending upon the frequency of the applied voltage. At low frequencies the electrons can respond fast enough to changes in the gate voltage, so the dielectric thickness once again becomes the insulator thickness, and the capacitance is once again independent of the applied voltage and equal to C_{ins}.

At higher frequencies the minority carriers cannot respond fast enough to changes in the gate voltage, so the capacitance is again the series combination of C_{ins} and C_D given in Equation 4.11. Further increases in gate voltage in this region result in the conduction band crossing the Fermi level and the onset of strong inversion. The depletion layer width now reaches a maximum, hence the capacitance reaches a minimum value and remains constant with further positive changes in gate voltage.

4.4.4. Interface Trapped Charge (Q_{it}, D_{it})

Interface trapped charge is present at the interface between the semiconductor surface and the insulating material, as shown previously in Figure 4.8. In conventional electronic theory the origin of this charge is due to the structural defects that are present in the lattice structure at the interface of the silicon and silicon dioxide insulator.

When considering the structure of MIM PMDs however, this semiconductor-insulator interface is never present. Firstly, in all cases these PMDs consist of a metal-insulator-metal structure, so this immediately rules out the possibility of interface trapped charge being present, as there is no semiconductor-insulator interface. Secondly, even if a semiconductor is used, the insulators used are polymer materials, which are not thermally grown as silicon dioxide is. This means that there is no lattice damage to the silicon, and any trapped charge present in the polymer insulator is likely to respond as insulator trapped charge. For these reasons any experiments relating to interface trapped charge will not be relevant when considering actual memory devices, hence interface trapped charge will not be investigated further.

4.4.5. Insulator Charges (Q_f, D_f; Q_{inst}, D_{inst}; Q_m, D_m)

The remaining types of charge shown in Figure 4.8 can be grouped together and classed as insulator charges. Fixed insulator charge, Q_f, is present in the insulating material, close to the semiconductor-insulator interface (within 30Å for Si-SiO_2 [111]), and as the name suggests it is immobile.

Insulator trapped charge, Q_{inst}, and mobile charge, Q_m, are both present in the bulk of the insulating material. Insulator trapped charge can either be introduced into a device during manufacture, or can be the result of charge being trapped in the insulator during normal operating conditions due to electrons and holes being injected into the insulator from the gate or substrate. Mobile ionic charge is present due to impurities in the insulating material. When SiO_2 is used as the insulating material the main causes of mobile charge are the ionic impurities Na^+, Li^+ and K^+, with sodium ions being the dominant impurity due to their high mobility in silicon dioxide and their abundance in the environment [127]. It is also likely that sodium will be the main contaminant in polymer insulators.

Any of the insulator charges that are present at the semiconductor-insulator interface will cause a shift along the voltage axis in the *C-V* curve with respect to the theoretical curve, so:

$$V_{FB} = \phi_{MS} - \left(\frac{Q_f + Q_{inst} + Q_m}{C_{inst}}\right) \qquad \textbf{Equation 4.12}$$

If the effect on the *C-V* curves of these charges are considered separately, then it is possible to design experiments that can individually measure each of the charge types.

Due to the different origins, and positions in the capacitor of Q_f, Q_{inst} and Q_m they will all respond differently when the capacitor is subjected to different voltage stressing conditions. These different behaviours are illustrated in Figure 4.14.

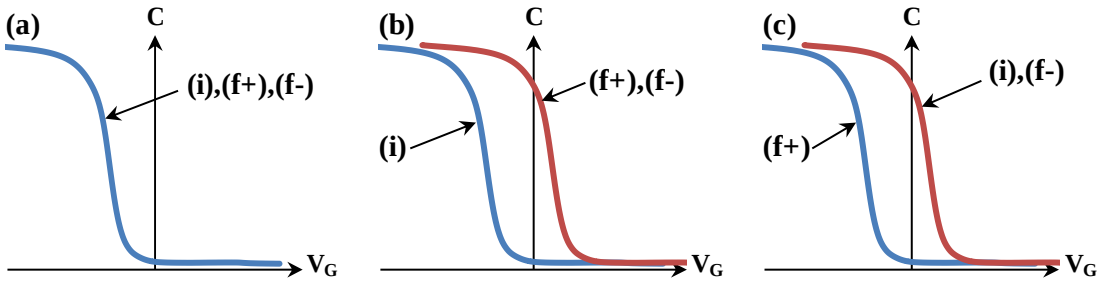


Figure 4.14 *C-V* curve shift under voltage stressing conditions due to; (a) Fixed insulator charge, Q_f. (b) Insulator trapped charge, Q_{inst} and (c) Mobile charge, Q_m. (i) denotes the initial curve, (f+) and (f-) after positive and negative voltage stress respectively.

For the case of Q_f, as it is immobile, stressing at either voltage polarity has no effect on the position of the charge, hence the curves remain the same under all stressing conditions (Figure 4.14(a)). Oxide trapped charges (in the case of SiO_2) tend to anneal out at reasonably low temperatures, stressing at either polarity results in a shift in the *C-V* characteristic towards the theoretical curve (Figure 4.14(b)). The voltage independence also suggests that while these charges are uniformly distributed throughout the insulator, they are immobile. Finally mobile charge will respond by drifting through the insulator depending upon the polarity of the electric field (Figure 4.14(c)). As discussed earlier the mobile ions will likely consist of predominantly Na^+, so under a negative gate bias will drift towards the gate electrode where they have no effect on the flatband voltage and a curve closer to the theoretical one results. Positive stressing moves the ions to the semiconductor interface, where they have maximum effect and result in a large shift in the *C-V* curve.

In conventional SiO_2 insulators this voltage stressing is usually performed at several hundred degrees Celsius and with a stressing voltage chosen to give an electric field across the insulator of a few $MV \cdot cm^{-1}$ [128]. This is obviously not possible with polymer insulators, however, it was found that by stressing at similar voltages at room temperature the expected shifts in the *C-V* curve still took place. After stressing for 30 minutes the *C-V* curves reached new equilibrium positions, with results from a typical device shown in Figure 4.15.

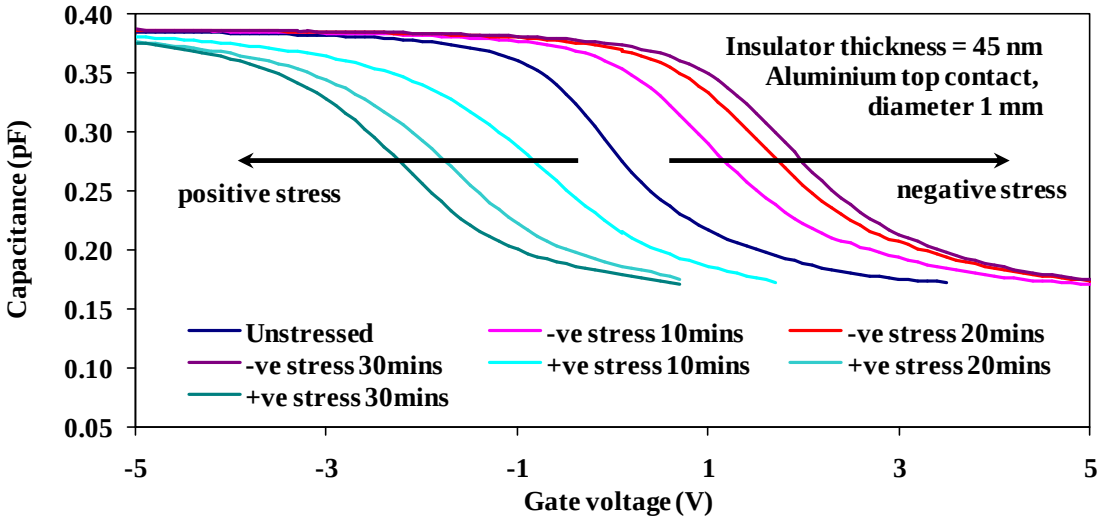


Figure 4.15 *C-V* curve shifts as a result of voltage stressing.

Both Q_m and Q_{inst} can be related to magnitude of the flatband voltage shift according to the equations:

$$Q_m = -\Delta V_{FB} \times C_{ins} \qquad \textbf{Equation 4.13}$$

$$Q_{inst} = -\Delta V_{FB} \times C_{ins} \qquad \textbf{Equation 4.14}$$

The results shown in Figure 4.15 match closely with the theoretical curves from Figure 4.14(c), leading to the conclusion that the mobile ions are responsible for the flatband voltage shift. Any contribution from Q_{inst} that is present is, in effect, masked by a much larger contribution from Q_m.

In order to measure the charge present that can be attributed to Q_f, firstly the contributions from Q_m and Q_{inst} have to be minimised as much as possible. By measuring the flatband voltage after the capacitor has been stressed at a negative voltage, mobile charges will be moved to the gate interface and their contribution will be minimised. Insulator trapped charge is immobile, so cannot be reduced this way. It is likely that the only way to reduce Q_{inst} is by performing anneals on the polymer film, which will also affect the magnitude of Q_f. Hence both Q_f and Q_{inst} have to be analysed together, however, as Q_f is close to the semiconductor-insulator boundary this will contribute the majority of the flatband voltage shift with only the portion of Q_{inst} near the semiconductor-insulator boundary contributing to the shift. Equation 4.12 can then be rewritten in terms of Q_f and Q_{inst}:

$$Q_f + Q_{inst} = (\phi_{MS} - V_{FB}) \times C_{ins} \qquad \textbf{Equation 4.15}$$

4.5. MIS Capacitance – Voltage Characteristics

4.5.1. Flatband Voltage and Flatband Capacitance Calculations

Equation 4.13 – Equation 4.15 all require a measurement of the flatband voltage in order to calculate the magnitude of the charges. In the case of Q_m and Q_{inst} only the change in flatband voltage is required, so as long as the *C-V* curves do not show any stretch-out effects, any arbitrary value can be used for the flatband capacitance. However, for Q_f an absolute value for V_{FB} is needed. Initially graphical methods were investigated for calculating the flatband voltage. By taking the second derivative of the function:

$$\frac{1}{\left(C_{hf}/C_{ins}\right)^2} \qquad \textbf{Equation 4.16}$$

A peak should then be present that corresponds to the flatband voltage of the capacitor [128]. However, due to the non-ideal characteristics of the polymer capacitors and the amount of noise that this method can introduce into the data, when this method was used, in many cases it became difficult to determine the exact position of this peak.

Due to the problems encountered with this method, the theoretical semiconductor equations were instead used to calculate the value of the flatband capacitance and hence find the flatband voltage. By utilising [111]:

$$C_{FB} = \frac{\varepsilon_{ins}\varepsilon_0}{t_{ins} + (\varepsilon_{ins}/\varepsilon_s)L_D} \qquad \textbf{Equation 4.17}$$

Where ε_s is the relative permittivity of silicon, and L_D is the Debye length, as defined by [128]:

$$L_D = \sqrt{\frac{kT\varepsilon_s\varepsilon_0}{eN_A}} \qquad \textbf{Equation 4.18}$$

This means that to accurately calculate C_{FB} the doping density of the silicon, N_A needs to be known. From the manufacturers specifications the resistivity of the silicon used in all the experiments was in the range of 1 – 10 Ω·cm, yet this could still mean a possible doping density of between approximately $1.3\text{x}10^{15}$ cm^{-3} and $1.5\text{x}10^{16}$ cm^{-3} [111]. However, it is also known that at high frequencies the measured capacitance will reach a minimum value when the depletion width is at a maximum, with the maximum depletion width, W_m given by [111]:

$$W_m = \sqrt{\frac{4kT\varepsilon_s\varepsilon_0 ln(N_A/n_i)}{eN_A}} \qquad \textbf{Equation 4.19}$$

With n_i being the intrinsic carrier concentration of silicon. By measuring the capacitance in depletion, the depletion layer capacitance, and hence the depletion width can be obtained from Equation 4.7 and Equation 4.11. The use of this method gives a doping density in the silicon of ~1.5x10^{16} cm^{-3}, which is in agreement with the manufacturers stated resistivity. Figure 4.16 shows the calculated curve for this doping density using Equation 4.17, with these values being used in all subsequent data analysis for calculating C_{FB} and V_{FB}.

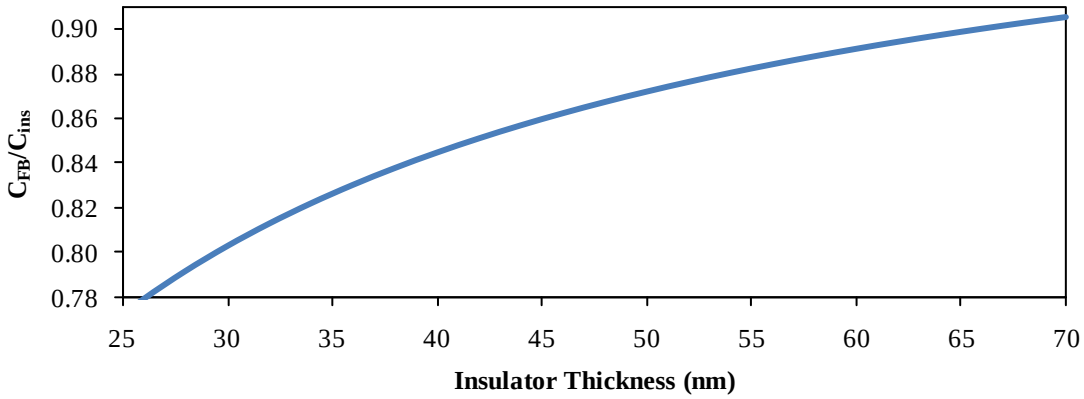


Figure 4.16 Normalised flatband capacitance vs. insulator thickness for polystyrene insulator and silicon doping density, N_A = 1.5x10^{16} cm^{-3}.

Now that the doping density of the silicon is known it is also possible to calculate an accurate value for ϕ_{MS} that will be used in the analysis of the various charge densities in §§4.5.2 – 4.5.3. By using theoretical values and basic semiconductor equations to calculate the value of ϕ_F, Equation 4.8 becomes:

$$\phi_{MS} = \phi_M - \left(\chi_s + {}^{E_g}/_2 + \phi_F\right)$$

$$= 4.28 - \left(4.05 + {}^{1.12}/_2 + 0.37\right)$$

$$= -0.70V$$

4.5.2. Mobile Ionic Charge

Mobile charge was investigated by fabricating several geometrically identical MIS capacitor structures, but with the polystyrene layer annealed at different temperatures. The same procedure as for the MIM dielectric strength experiments (§4.3.1) was followed with anneal temperatures ranging from 30 °C to 120 °C in 15 °C intervals. Nominal dimensions of the capacitors were a 45nm polystyrene layer, with 1mm diameter gate contacts. As discussed in §4.4.5 all stressing took place at room temperature, with stressing voltages of ± 4.5 V used to give an electric field of approximately 1 MV·cm^{-1}.

The calculated values of mobile charge density as a function of the polystyrene anneal temperature can be seen in Figure 4.17.

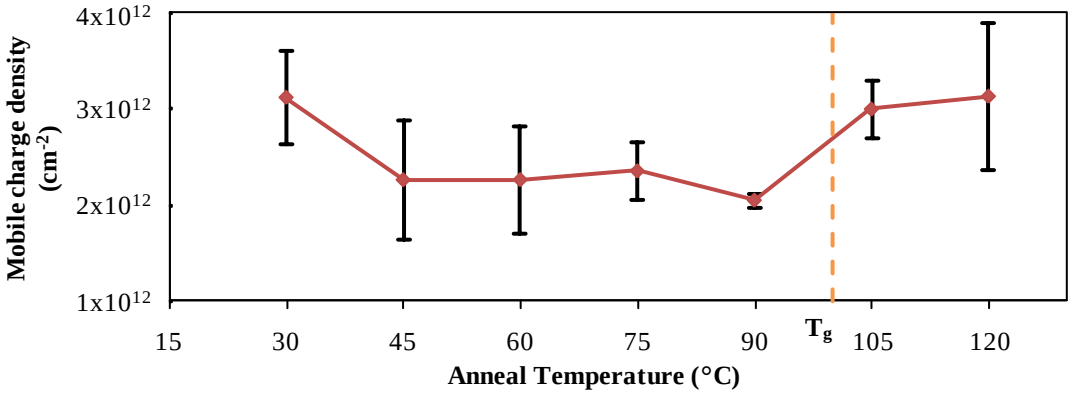


Figure 4.17 Mobile charge density vs. anneal temperature.

Across all the samples tested this equates to an average mobile charge density of 2.6×10^{12} cm^{-1}. This compares well with measured charge densities in conventional SiO_2 MIS capacitors [127], which would be expected, as the main source of contaminant ions comes from environmental factors, such as solvents and human contact rather than any source that is inherent to a specific process or material.

It can be seen that mobile charge density is reasonably constant as anneal temperature is increased, with a slight trend towards decreasing mobile charge density at higher anneal temperatures, until the point of T_g is reached. Considering the origin and nature of mobile charges they should not be annealed out at elevated temperatures, and would in fact be expected to remain constant. However, as previously discussed in §4.4.5 in experimental capacitors the effects from other types of trapped charge will also be present to some degree, despite any attempts to minimise the charges that are not being studied. The apparent decrease in mobile charge density up to the value of T_g could be a contribution from either fixed or insulator trapped charges that are present near the semiconductor-insulator interface. It also has to be noted that the size of the error in the measured data is relatively large, as is evident from the error bars in Figure 4.17, and hence it is more likely that the apparent decrease in Q_m could simply be due to the size of the error in the data.

4.5.3. Fixed & Insulator Trapped Charge

Fixed and insulator trapped charge were investigated by measuring capacitors with the same specification as those for mobile charge. To minimise the influence on the flatband

voltage from Q_m the capacitors were stressed with a negative gate bias for 30 minutes to move any mobile ions away from the semiconductor-insulator boundary.

The flatband voltages of the capacitors were then measured and Equation 4.15 used to calculate the magnitude of trapped charge. As previously described in §4.4.5 the measured charge will be a combination of Q_f and any Q_{inst} that is present near the semiconductor-insulator boundary. As the polystyrene insulator layer should be homogenous throughout its entire thickness (i.e. it is not structurally different at the semiconductor boundary in the same way that $Si0_2$ is), it is reasonable to assume that Q_f and Q_{inst} are of the same origin in the polymer film and can be treated as an immobile charge that is uniformly distributed throughout the polystyrene. For this reason, both types of charge will be grouped together and described as fixed charge, Q_f.

Figure 4.18 shows the measured levels of fixed charge density.

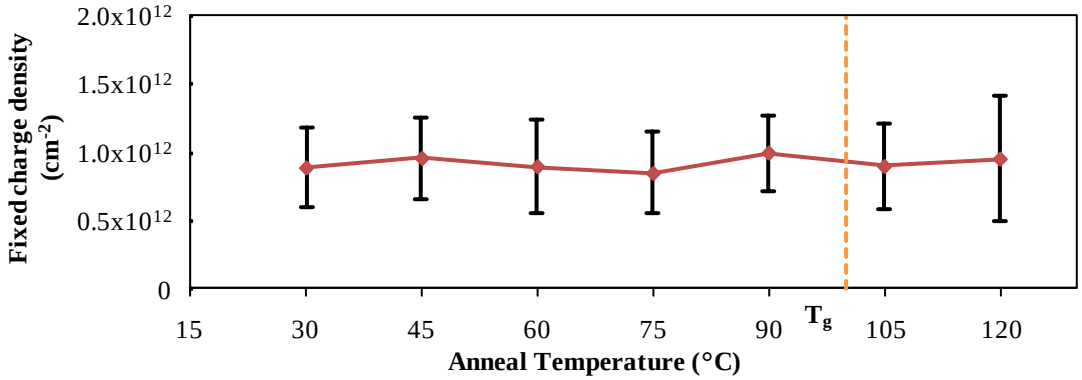


Figure 4.18 Fixed charge density vs. anneal temperature.

It can be seen that fixed charge remained approximately constant as the anneal temperature was increased, with an average fixed charge density of ~$9.2x10^{11}$ cm^{-1} calculated across the whole range of anneal temperatures. For all anneal temperatures it was found that the effects of fixed charge resulted in a shift in the *C-V* curves towards positive voltages. This indicates that the fixed insulator charge in polystyrene is negative, which differs from conventional fixed charge in $Si0_2$ where the fixed charge near the semiconductor-insulator interface is generally positive [111].

4.6. Summary of Chapter 4

In this section, justifications for the use of polystyrene as the insulating polymer matrix in PMDs have been discussed.

Important characteristics for the fabrication quality of the polymer layers in PMDs, such as the spin-coating parameters and the factors affecting the quality of the polystyrene layer have been identified and optimised. Post optimisation, the dielectric strength of polystyrene was found to greatly exceed the expected bulk material value, though this phenomenon has also been reported by other research groups and can be explained by considering the lower density of defects that are likely present in the thin film material studied. It was found that dielectric strength had a dependence on both the film thickness and polymer anneal temperature, with the highest dielectric strengths resulting from an anneal at slightly below the glass transition temperature of polystyrene. The conduction mechanism for polystyrene has also been investigated and identified as likely being dominated by contact limited Schottky emission.

Levels of trapped charge in the polystyrene films were studied using techniques similar to those used for conventional inorganic insulating materials, but with the necessary modifications to the techniques to account for the low temperatures and voltages that polystyrene can withstand. Levels of both mobile and fixed trapped charges in the polystyrene were found to be comparable to those in conventional inorganic insulators, showing that polystyrene is a good candidate for use in organic electronic devices.

As discussed at the beginning of Chapter 4, there was a large gap in knowledge concerning the electrical properties of polystyrene thin films. This knowledge gap has now been filled allowing polystyrene to be used as the insulating material in the memory devices and test structures fabricated in the subsequent chapters.

CHAPTER 5

Investigating the Theorised Memory Mechanisms Responsible for the Conductivity Change in Polymer Memory Devices

"The universe is full of magical things patiently waiting for our wits to grow sharper"

...Eden Phillpotts

This chapter focuses on providing scientific experimental data regarding the theories that have been proposed to explain the change in conductivity of PMDs. Data is also presented regarding the electrical characteristics of the constituent materials of gold nanoparticle PMDs and discussions follow regarding how this data helps in elucidating the mechanisms responsible for the PMDs' change in conductivity.

5.1. Polystyrene Insulator Trapped Charges

The possibility that impurities or trapped charges that are present in the polymer layer could be responsible for the change in conductivity in PMDs is an area that has received little attention. While many devices have been based on polystyrene, until the studies conducted in Chapter 4, there was a fundamental lack of data regarding the electrical properties of ultra-thin polystyrene films. One of the main theories for the switching mechanism in gold nanoparticle PMDs is based on the charging of the nanoparticles under the application of an electric field. As such it is possible that if the density of intrinsic trapped charges in the polymer is sufficient, it could be these charges that are responsible for the conductivity change, rather than the deliberately introduced gold nanoparticles. The investigation in §4.5 showed that the levels of trapped charge that are present in the polystyrene are comparable to those found in other polymer insulator materials [129-130] and silicon dioxide [111].

While there have been reports of switching in insulating films dating back for several decades (see §2.2.1 for a discussion on resistive switching), these phenomena are not attributed to intrinsic trapped charges in the films charging and discharging. This puts switching in these insulating films closer to the category of RRAMs where insulator breakdown and filamentary conduction are likely mechanisms. This in itself is strong evidence that the intrinsic trapped charges in polystyrene are not responsible for the switching behaviour of polystyrene based PMDs.

The investigation in §4.5 also revealed that mobile insulator trapped charges were present in the greatest density compared to fixed insulator charges, which may indicate that mobile charge will have the larger influence on electrical characteristics. It was also shown in §4.4.5 that mobile insulator trapped charges can move through the polymer layer at room temperature, but the process took approximately 30 minutes to move charges through a 45 nm polystyrene film. This is many of orders of magnitude slower than the response of PMDs in literature, which have shown response times on the order of nanoseconds [9-10]. This rules out the possibility that the movement of mobile charges could be responsible for any change in conductivity.

Perhaps the strongest evidence though for the intrinsic trapped charges not being responsible for the change in conductivity comes from the experimental data that will be presented in §6.1.2. These results show that switching only takes place when gold nanoparticles are added to the polystyrene films. Adding other forms of charge trapping sites, such as 8HQ, did not result in reliable switching behaviour, signifying that the nanoparticles are the most important constituent for obtaining memory characteristics.

5.2. Nanoparticle Charging

There are many proponents of a memory mechanism based on the storage of charge by nanoparticles, or other charge trapping species in the PMD. Table 2.1 in §2.3.4 gives an overview of all the papers which cite this as being the likely mechanism. However, there are still many variations in the exact details of the mechanisms, with many discrepancies between different research groups, even for the same device structure studied.

There have been several reports in literature of nanoparticle charging experiments conducted via scanning tunneling microscopy [131-134], with most papers demonstrating a coulomb blockade effect at room temperature and phenomena known as a coulomb staircase, as will be discussed in greater detail in §5.2.2. There has been significantly less work published using other methods that could detect the charging of nanoparticles, such as electrostatic force microscopy and device based measurements where the nanoparticles are unambiguously responsible for any changes in properties. As a result of this lack of data there are still unanswered questions concerning the charging of the nanoparticles in relation to real world devices, and even whether nanoparticle charging is possible when they are integrated into memory devices. This section aims to conduct charging experiments of nanoparticles

using a variety of different techniques including STM (§5.2.3), EFM (§5.2.4), oscilloscope time constant measurements (§5.2.5) and MIS capacitor based measurements (§5.2.6).

5.2.1. LB layer Deposition Theory and Optimisation

Many of the experimental techniques used in the section require controlled and precise deposition of gold nanoparticles. One technique that is perfectly suited to this is Langmuir-Blodgett deposition [135-137], where monolayers of materials can be deposited on substrates in a highly controlled manner. The basic theory behind LB deposition is that a monolayer of the substance to be deposited is floated on top of a liquid subphase. This is usually done by dissolving the material in a solvent and dropping a small amount (10 – 40 µl) on to the subphase. The solvent then evaporates leaving the deposition material behind, spreading out to form a monolayer. Substrate material is then vertically passed through the deposition material, with transfer of the monolayer from the subphase to the substrate taking place, as shown in Figure 5.1.

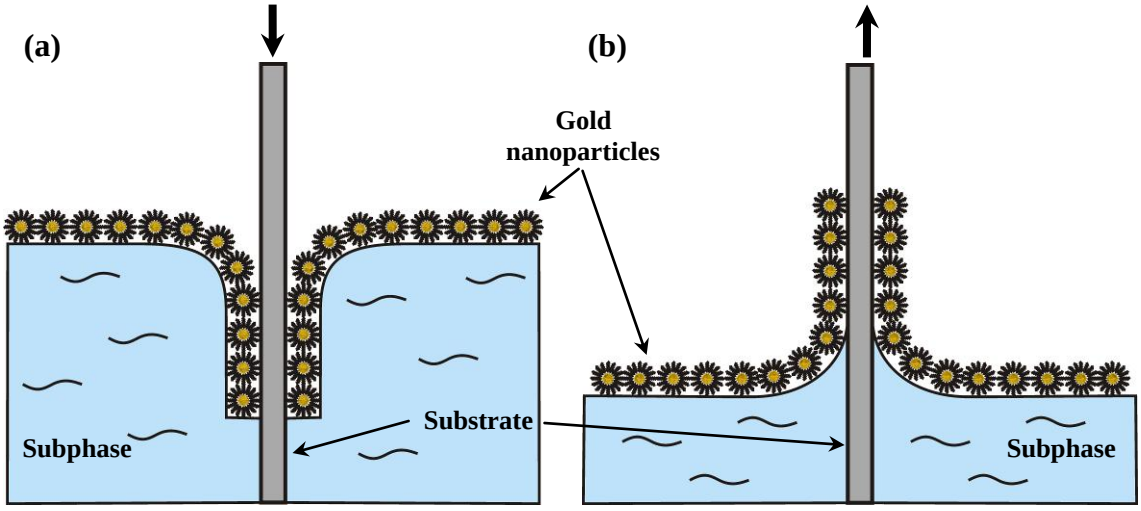


Figure 5.1 Schematic of LB deposition of gold nanoparticles onto a substrate. (a) X-type transfer. (b) Z-type transfer

This process takes place in a Langmuir-Blodgett trough, as shown in Figure 5.2, with the barriers acting to compress the deposition material to a certain surface pressure, as measured with the Wilhelmy plate and microbalance.

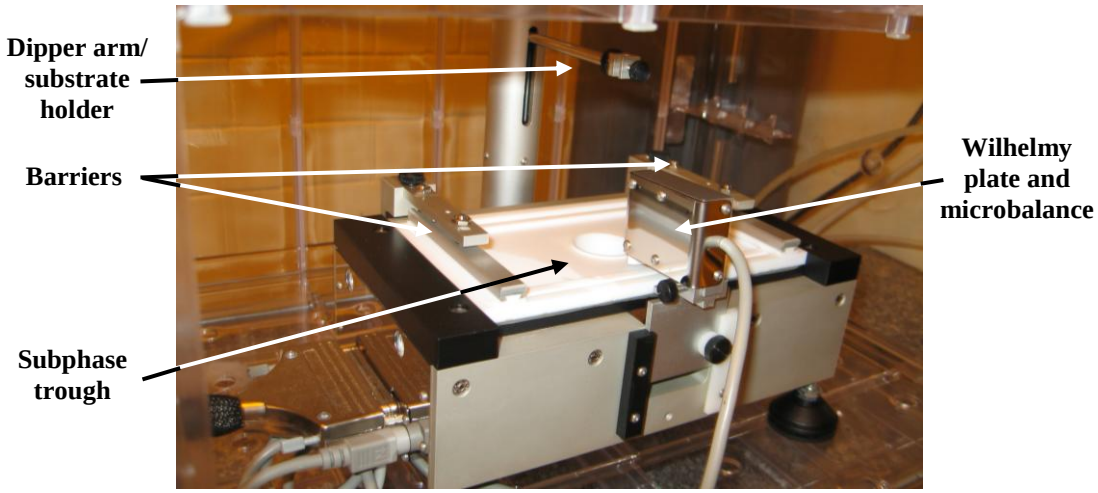


Figure 5.2 Molecular Photonics model LB715 Langmuir-Blodgett trough.

In theory the deposition material will go through several phase transitions as it is compressed by the barriers, called the gaseous (G), expanded (E) and condensed (C) phases, which can be compared to the gaseous, liquid and solid phase of conventional materials. For a typical material that is used for LB deposition, such as the long chain fatty acid, icosanoic acid ($C_{19}H_{39}COOH$) these three phases result in a surface pressure vs. area per molecule isotherm such as that shown in Figure 5.3(a).

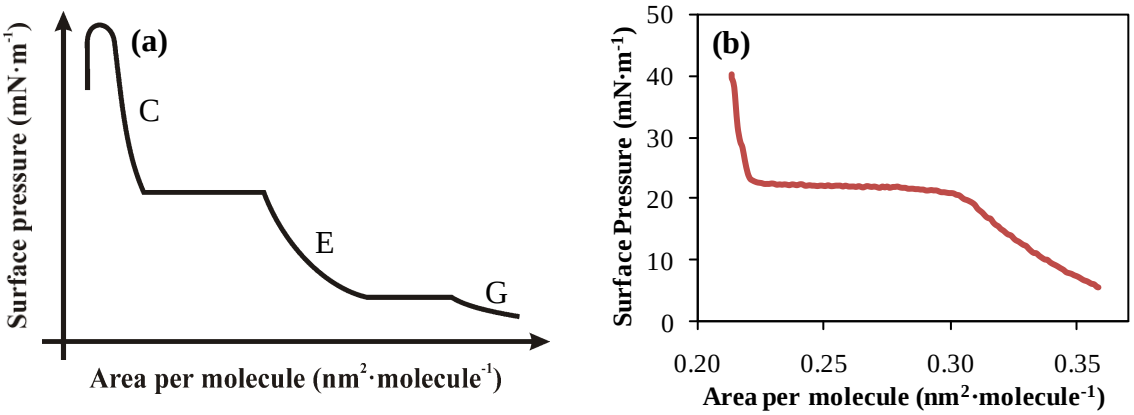


Figure 5.3(a) Ideal surface pressure vs. area isotherm for icosanoic acid. (b) Measured isotherm for icosanoic acid at 20°C.

The condensed phase coincides with the point where the molecules are tightly packed on the surface of the water, hence the area per molecule is roughly equal to the cross sectional area of the molecule (0.19 nm^2 for icosanoic acid [137]). In order to be able to form the initial monolayer on the subphase the deposition material and the subphase have to be immiscible. During the course of this research two types of gold nanoparticle have been used; Type-I and Type-II nanoparticles. Both types have capping ligands based on hydrocarbon molecules,

making the nanoparticle as a whole hydrophobic in nature, hence they readily form monolayers on a water subphase making them suitable for LB deposition. The specifications for the two different nanoparticle types can be found in Appendix D.

Particular care has to be taken to ensure impurities are not present in the monolayer during deposition, the main sources of impurities are the subphase liquid, solvents and human contact. In all experiments deionised water (resistivity >18 MΩ·cm) was used as the subphase liquid, with low residue, or electronic grade solvents used wherever possible to disperse the nanoparticles in. Prior to the deposition material spreading, any surface contaminants on the water were also compressed to the centre of the trough and removed with a glass capillary tube. This process was repeated until the surface pressure remained constant with trough area, indicating that all surface contaminants had been removed.

Typical surface pressure vs. trough area for both Type-I and Type-II gold nanoparticles are shown in Figure 5.4(a) and (b) respectively.

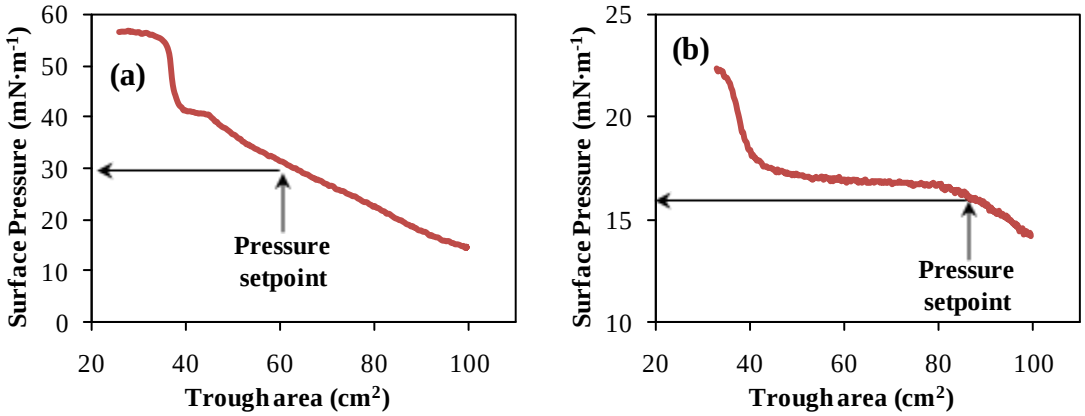


Figure 5.4 Surface pressure vs. trough area isotherms for; (a) Type-I and (b) Type-II gold nanoparticles.

The usual practice of plotting surface pressure against area per molecule for the nanoparticles was not possible in this case, as density information is needed for an accurate calculation of the area per molecule. Because density information was not available for either type of nanoparticle, the trough area was used in lieu of the area per molecule. For both types of nanoparticle it was found that the phase transitions were not as obvious as for icosanoic acid, with successful deposition taking place for the nanoparticles in the region that, from the isotherms, appears to be their expanded phase. This corresponded to surface pressures from 30 – 35 $mN \cdot m^{-1}$ for Type-I nanoparticles and pressures of 15 – 18 $mN \cdot m^{-1}$ for Type-II nanoparticles. It was found that for surface pressures below these values transfer to the substrate did not occur, while for higher pressures monolayer collapse occurred and it was not possible to hold the set point pressure.

The speed that the substrate moves through the monolayer can also play an important role in the quality of the deposited films, with the dipper having to move slowly enough to allow the nanoparticles that are being deposited to be replaced by the compression of the barriers. For both types of nanoparticles, slower dipper speeds were found to result in better quality depositions, with dipper speeds of 3 – 10 $\mu m \cdot s^{-1}$ used for all depositions. In all cases Type-I nanoparticles were found to deposit on the downward substrate stroke only, resulting in X-type deposition, with a typical deposition characteristic shown in Figure 5.5(a). The presence of a single monolayer was confirmed from AFM images of the substrates indicating that the decrease in trough area on the upward stroke is due to the sinking of these nanoparticles through the subphase or the collapse of the monolayer over time. For the Type-II nanoparticles deposition could either be X-type or Z-type, with a typical deposition characteristic shown in Figure 5.5(b).

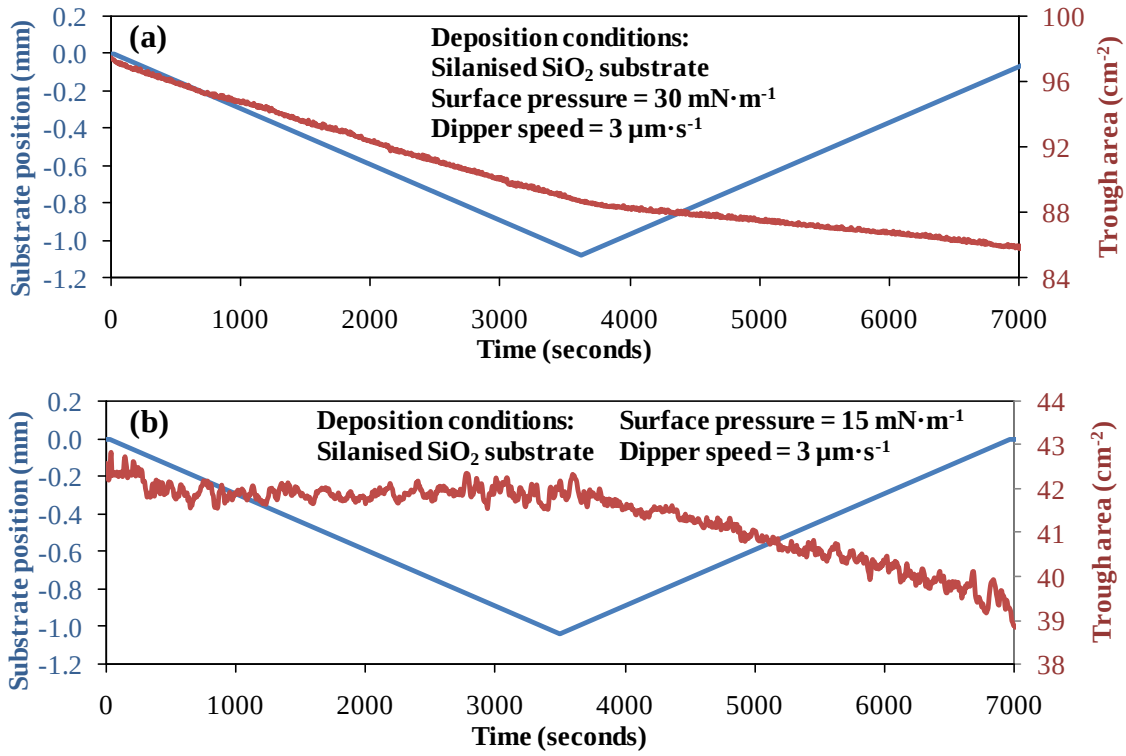


Figure 5.5 Typical area vs. time graphs for (a) Type-I gold nanoparticles and (b) Type-II gold nanoparticles.

Exact transfer ratios for each deposition could not be accurately determined, in part due to cleaved silicon being used as the basis of many of the substrates, so the exact substrate size was not known. It is also in part due to the likelihood of partial (if not complete) deposition taking place on the reverse of the substrate. Subsequent AFM images of depositions could give estimates of transfer ratios, with optimised deposition conditions for Type-II gold

nanoparticles resulting in >85% coverage for SiO_2 substrates, >99% coverage for evaporated gold substrate and >97% for flame annealed gold substrate. (See Appendix H).

5.2.2. Coulomb Blockade Overview

The most extensive form of nanoparticle charging that has been studied is the phenomenon of Coulomb blockade. If the case shown in Figure 5.6(a) is considered, where an STM tip is positioned above a gold nanoparticle, which is in turn deposited on a conducting substrate, it is possible for electrons to tunnel onto the nanoparticle when a voltage is applied to the STM tip and in certain circumstances become trapped there, as illustrated by the band diagram in Figure 5.6(b).

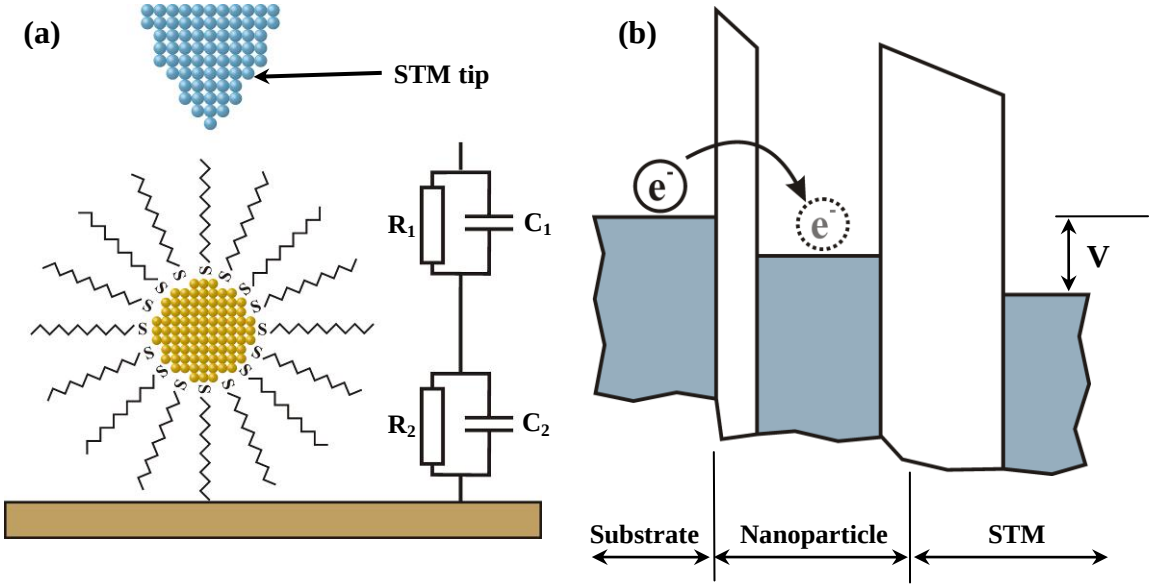


Figure 5.6(a) Double barrier tunnel junction formed when an STM tip comes in close proximity with a nanoparticle. (b) Band diagram when a voltage is applied to the STM tip.

Once an electron has tunneled onto the nanoparticle, Coulomb repulsion will then prevent the tunneling of a second electron, resulting in Coulomb blockade. By considering the double junction system it is possible to define several parameters, firstly the capacitance of the nanoparticle can be modelled as a conducting sphere surrounded by an finite insulating shell (corresponding to the gold core and capping ligands) which is given as [138-139]:

$$C_{NP} = 4\pi\varepsilon_0\varepsilon_r\left(\frac{r}{d}\right)(r+d) \qquad \textbf{Equation 5.1}$$

Where ε_r is the dielectric constant of the capping ligands, r is the radius of the nanoparticle core and d is the thickness of the ligand shell. Alternatively the capacitance may be simply modelled as a conducting sphere in a dielectric material, given by:

$$C_{NP} = 4\pi\varepsilon_0\varepsilon_r r \qquad \textbf{Equation 5.2}$$

The true capacitance will be estimated to be the average given from the two methods. It is also possible to define the time taken to charge the nanoparticle as the time constant of the system:

$$\tau = R_t C_{NP} \qquad \textbf{Equation 5.3}$$

Also the voltage required to transfer an electron to the nanoparticle is:

$$V = \frac{e}{C_{NP}} \qquad \textbf{Equation 5.4}$$

and the energy (in Joules) required to charge the nanoparticle is given by:

$$E = \frac{e^2}{2 \times C_{NP}} \qquad \textbf{Equation 5.5}$$

For Coulomb blockade to take place there are two criteria that need to be satisfied, firstly the charging energy of the nanoparticle has to be greater than the thermal energy, so at room temperature this requires that E >> 26 meV. Secondly the Heisenberg uncertainty principal states that:

$$\Delta E \Delta\tau \geq \frac{h}{2} \qquad \textbf{Equation 5.6}$$

Where h is Planck's constant. This puts a lower limit of the values of the tunnel resistances of ~25.813 kΩ, referred to as the von Klitzing constant.

In the case where $R_1C_1 = R_2C_2$ from Figure 5.6 then the electron is equally likely to tunnel off the nanoparticle to the STM tip. However, if there is a large asymmetry in the tunneling barriers then the probability of an electron tunneling onto the nanoparticle from the substrate is greater than the probability of the electron tunneling from the nanoparticle to the STM tip. In this case an integer number of electrons can be confined on the nanoparticle depending upon the applied voltage with the *I-V* characteristics showing a distinctive Coulomb staircase effect, as illustrated in Figure 5.7. Each step corresponds to the addition of one extra electron to the nanoparticle, with a spacing along the voltage axis equal to the voltage required to transfer an electron to the nanoparticle from Equation 5.4.

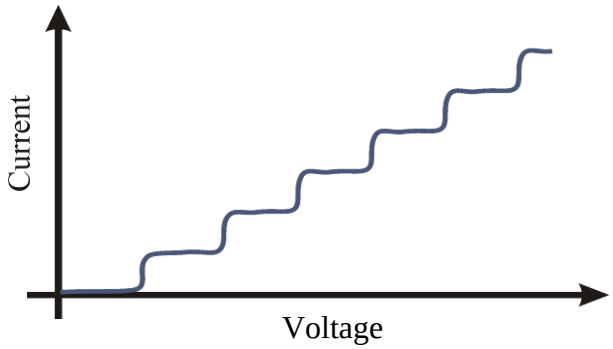


Figure 5.7 Coulomb staircase effects in the current–voltage characteristic of the gold nanoparticle.

5.2.3. STM Charging Experiments.

In order to show that it is possible for charging of gold nanoparticles to take place experiments were conducted to replicate the coulomb blockade effects, that have been demonstrated in other nanoparticle systems [131-134]. The first process is to confirm that the gold nanoparticles used are capable of showing Coulomb blockade at room temperatures. To do this the two criteria discussed in §5.2.2 have to be met. From Equation 5.1 and Equation 5.2 the capacitance of the Type-I nanoparticles used in the STM experiments can be estimated. The dielectric constants of the two types of capping ligands are 2.5 and 2.0 (see Appendix D), so for the purposes of the capacitance calculations an average value of 2.25 will be used, with a capping ligand length of 1.8 nm (the average length of the two ligands). From the nanoparticle diameter of 8 nm this would give a core diameter of 4.4 nm, and hence estimated capacitances of 1.5×10^{-18} F from Equation 5.1 and 6.6×10^{-19} F from Equation 5.2. Taking an average of these, of 1.1×10^{-18} F, results in a charging energy of ~75 meV. The second condition that has to be met is a tunnel resistance greater than the von Klitzing constant. This is more difficult to confirm from simple calculations, but similar work has shown similar chain length capping ligands to have tunnel resistances in the range of hundreds of megaohms to several gigaohms [140]. Both these values are orders of magnitude higher than the von Klitzing constant, so it is likely that the Type-I gold nanoparticles will also have tunnel resistances larger than required. From the calculated capacitance of the nanoparticles, and from Equation 5.4 it would be expected that the voltage required to charge the nanoparticle with one electron is ~150 mV, so if a Coulomb staircase is present each step will occur at a spacing of 150 mV along the voltage axis.

Initial STM experiments were conducted in a custom-made ultra-high-vacuum STM system (UHV-STM) [141] at the National Physical Laboratory (NPL) [142]. All experiments were conducted at pressures below 5×10^{-9} Torr and at room temperature.

Substrate materials were fabricated by thermally evaporating a 50 nm thick gold film onto clean silicon. Gold nanoparticles were then deposited onto the gold by LB deposition of Type-I nanoparticles with a thickness of two monolayers. STM investigations of the sample surface were then undertaken, with the aim of identifying areas of nanoparticles on the surface on which *I-V* measurements could be taken. Typical STM images are shown in Figure 5.8(a) and (b).

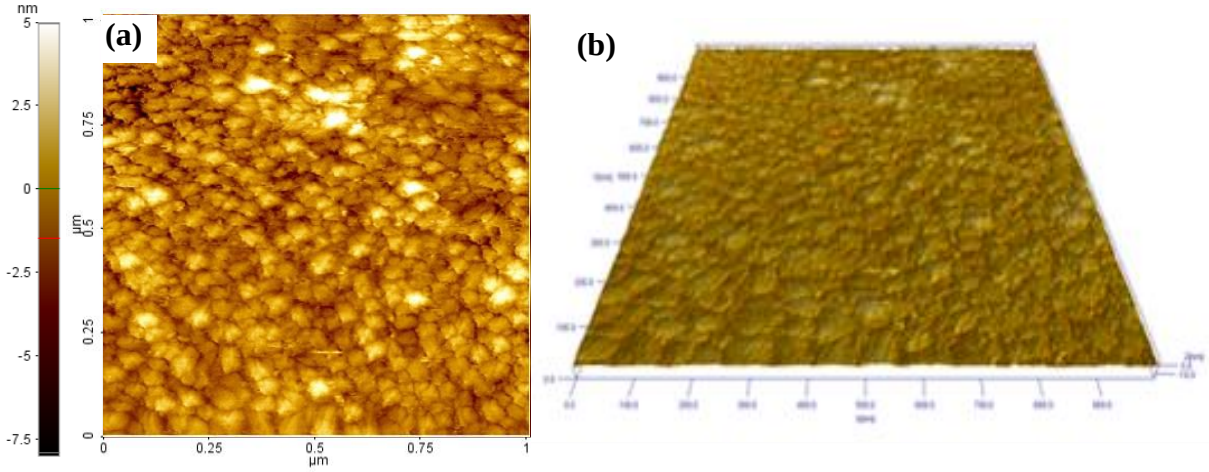


Figure 5.8 STM image of the gold substrate with LB deposited Type-II nanoparticles. (a) Topography and (b) 3D topography.

Here it is possible to see the grain structure of the evaporated gold layer, but there does not appear to be any evidence of gold nanoparticle deposition. From other images of LB deposited gold nanoparticles (such as those shown in Appendix H), unless a step at the edge of the monolayer is present in the image, it can be difficult to tell from the surface morphology whether it is indeed the gold substrate that is being imaged, or the monolayers of gold nanoparticles which are conforming to the topography of the substrate. In order to confirm the presence of nanoparticles on the surface several different techniques were used:

1. *I-V* curves were measured with the STM tip
2. Optical microscope images of the edge of the LB layer were captured
3. AFM images of the LB layer were taken.

An array of 25 *I-V* curves was measured at regular intervals over the 1 µm scan area of the STM image, with a typical characteristic shown in Figure 5.9. The characteristics were found to be approximately symmetrical, hence only the positive portion is shown. It was however found that there was a large amount of variability between the scans, with measured currents at 1 V ranging from 1 nA up to 100 nA (current limited by the instrumentation), with an average current at 1 V of ~18 nA, but a standard deviation of ~28 nA.

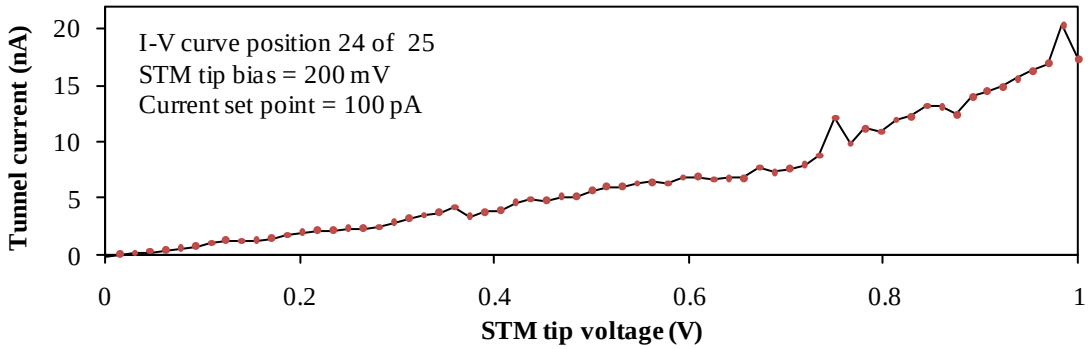


Figure 5.9 Typical *I-V* curve taken from the substrate area shown in Figure 5.8.

At low voltages the relationship is approximately linear, as would be expected for direct tunneling through a square barrier. There is also a general trend in the data to show deviation from a linear relationship for voltages > 0.7 V, possibly switching to Fowler-Nordheim tunneling (tunneling through a triangular barrier) (See §3.1 for a description of conduction mechanisms). However the variability between the data, and the amount of noise that is present in the *I-V* characteristics means it is not possible to confirm this hypothesis.

From optical microscope images of the edge of the LB nanoparticle layer (Figure 5.10(a)) it is clear that the deposition of nanoparticles is sporadic, with what appear to be conglomerations of nanoparticles separated by large undeposited areas. This is also confirmed by AFM topography images shown in Figure 5.10(b) and (c) taken with a Veeco Nanoscope III in tapping mode.

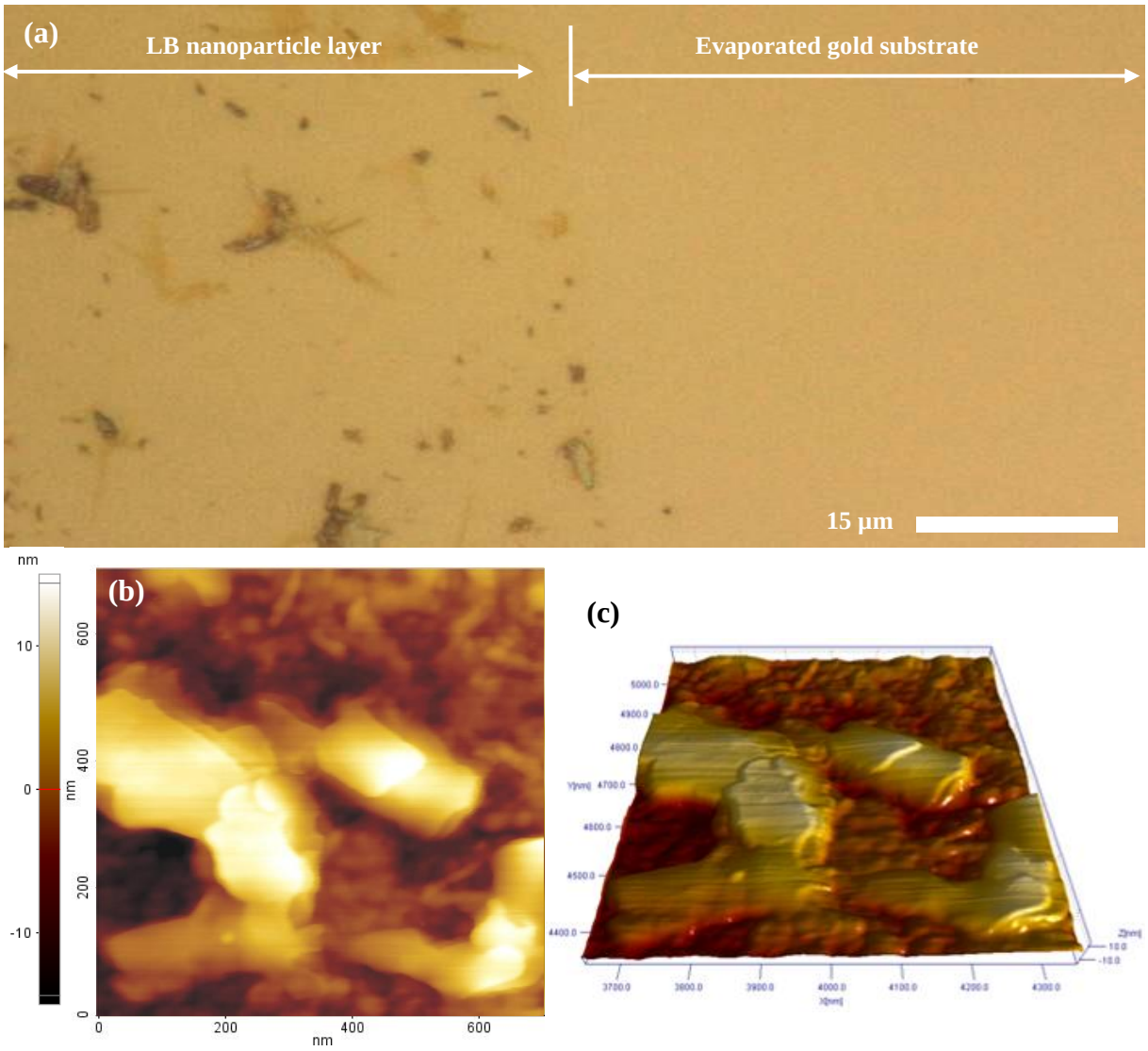


Figure 5.10(a) Optical image of the LB nanoparticle/substrate interface. (b) Topography AFM image of nanoparticle conglomerations. (c) 3D topography clearly showing the layer structure of the nanoparticle islands.

These images show a clear layered structure in the conglomerations indicating that these islands are indeed formed from nanoparticles. Analysis of line profiles revealed step heights between the layers of ~5 nm which is in good agreement with the size of the nanoparticles and previous investigations of layered structures in nanoparticles [143]. Between the islands there is no evidence for deposition of nanoparticles, indicating that the image in Figure 5.8 and the *I-V* characteristics taken are actually of the gold substrate, rather than a nanoparticle monolayer. Many separate attempts (~30) were made to withdraw the STM tip and re-engage in different areas of the substrate, however in all cases the same surface morphology as Figure 5.8 was found. Even though AFM images show that nanoparticles are present on portions of the substrate, STM limitations meant that in most cases an STM scan size of 1

μm^2 or less was used, resulting in a high likelihood that the STM always engaged the substrate in the areas between the nanoparticle islands.

In order to ensure that a guaranteed layer of nanoparticles was present on the substrate nanoparticles were also deposited using the drop casting method, with a nanoparticle concentration of 1 $mg \cdot ml^{-1}$ in chloroform used. A similar deposition technique has been used by O'Brien *et al*. [132] in a study using conducting-AFM measurements to measure Coulomb blockade on gold nanocrystal arrays. To obtain the electrical characteristics this technique relies on the STM tip penetrating the nanoparticles until the setpoint tunneling current is reached. The drawback of this technique is the difficulty in ensuring that the tip penetrates sufficiently to ensure the characteristics of a single nanoparticle are measured. It was not possible with this method to reliably image the surface, likely due to the fact that the tip was penetrating into the nanoparticle layer, however, *I-V* data could be obtained, once again with an array of 25 measurements taken in over a 1 μm^2 scan size.

A typical *I-V* characteristic for the drop-cast nanoparticle layer is shown in Figure 5.11(a), with only the positive portion shown due to the symmetry in the *I-V* curve. It was found here that the variability between devices was much reduced, with an average current at 1 V of ~11 nA, with a standard deviation of ~6 nA.

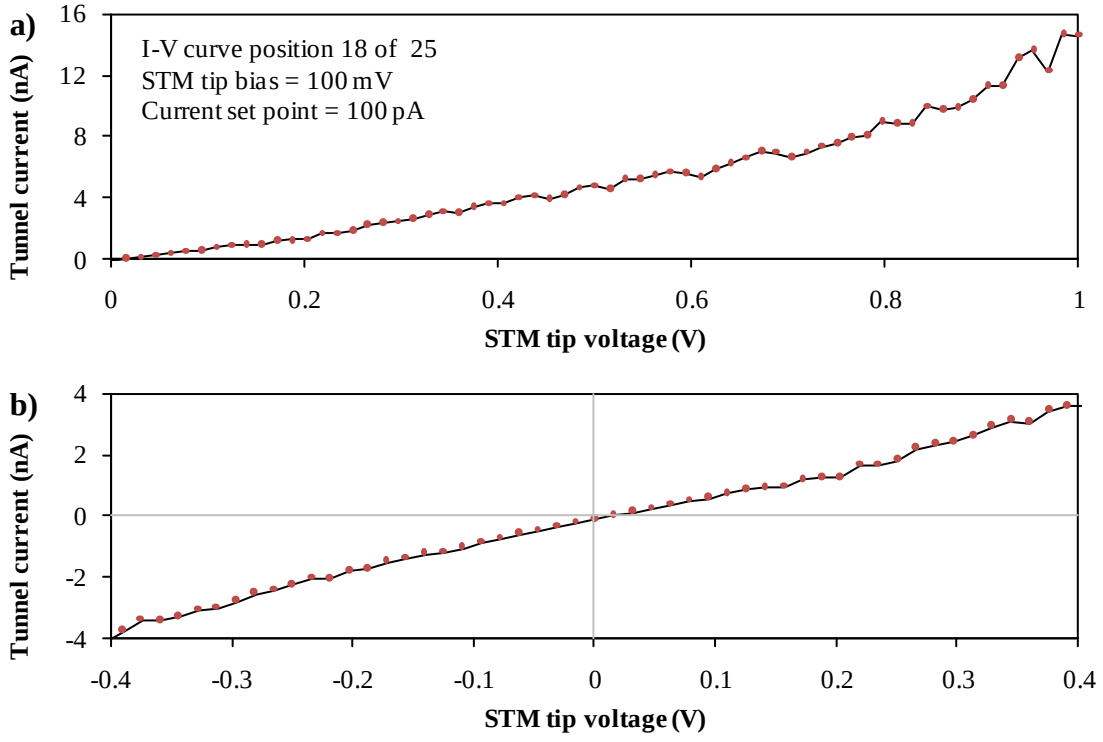


Figure 5.11(a) Typical *I-V* curve taken on the drop-cast nanoparticle layer. (b) Area around zero volts of the same curve in greater detail.

The majority of the *I-V* curves also showed evidence of possible step features or slight oscillations in the characteristic, with these steps present at a consistent spacing throughout all the characteristics. By taking the first derivative of the curves to find the peaks associated with each step, the average distance between each step was found to be ~50 mV, which is considerably less than the expected charging voltage of 150 mV for these nanoparticles. If the curves are examined in closer detail around zero volts (as shown in Figure 5.11(b)) it is also clear that there is no current blocking close to zero volts, as would be expected for Coulomb blockade. It should be noted that the resolution in the voltage axis is also not great enough to be able to rule out the possibility that the apparent steps are simply an artefact of the voltage step size (15 mV) used for gathering the *I-V* data. It is also not possible to rule out noise in the characteristics being responsible for the step features. From Figure 5.9 the *I-V* curves of the gold substrate also show a degree of noise, which would also be expected to be present in this data. The calculated charging energy for Type-I nanoparticles of 75 meV is greater than the thermal energy at room temperature, and as such Coulomb blockade would be expected. However, there are several possible reasons why a Coulomb staircase was not observed. Firstly, as the size of these nanoparticles is not precisely determined, and due to the assumptions made when calculating the nanoparticles' capacitance, it is possible that there could be a large amount of error in the charging voltage. Other studies using these types of nanoparticles have stated that the error in the size could be as great as 50% [87]. If this was the case, then the maximum nanoparticle size could be 12 nm diameter, which would result in a charging energy of ~19 meV, and no Coulomb blockade at room temperature. Secondly, as the nanoparticles were drop cast onto the substrate, it is possible that tunneling through several layers of nanoparticles took place, rather than a single nanoparticle. The *I-V* characteristics of several nanoparticles may not result in a Coulomb staircase, but would still be expected to show Coulomb blockade at low bias. Thirdly, in order to observe the Coulomb staircase there has to be a large difference between R_1C_1 and R_2C_2, which is not possible to confirm in the experiments here. For these reasons there has to be the conclusion that STM experiments on Type-I gold nanoparticles show no evidence of Coulomb blockade or nanoparticle charging.

5.2.4. Electrostatic Force Microscopy Charging Experiments

5.2.4.1. Electrostatic Force Microscopy on Polymer Films

With the use of EFM it is possible not only to image surface topography of a sample, as is the case with standard AFM, but also gather information about the electrostatic forces that are present on a surface. This technique was used by Ouyang *et al*. [9-10] as experimental evidence for the nanoparticles in the polystyrene matrix being charged due to a charge transfer between the 8HQ and the gold nanoparticles. Only limited information was presented, with large scale (>20 μm) EFM images being shown as supporting evidence. This means that only the overall effect of the polymer + nanoparticles + 8-hydroxyquinoline is measured. To be able to show that the nanoparticles themselves are being charged it would be necessary to image individual nanoparticles in the polymer matrix and show the contrast between the nanoparticles and the polymer, which would likely prove very difficult considering the size of the nanoparticles and the image resolutions achievable from EFM.

There are several reports of charging demonstrated in nanocrystals and nanoparticles embedded in insulating matrices, however these approaches all relied on the formation of metallic nanocrystals [144-145] or semiconducting nanocrystals [146-147] in a hard insulating oxide matrix (SiO_2 or HfO_2 for example). As such the nanocrystals were large enough to be imaged on an individual basis and quantitative analysis of the amount of charge held by individual nanocrystals could be made. These nanocrystals are however quite different in size and structure from the nanoparticles used in this investigation and by Ouyang *et al*. so it is unlikely that individual nanoparticles could be charged and imaged here for the following reasons:

- The size of the nanoparticles and spacing between them is likely to be below the resolution of the EFM images.
- The polymer matrix used here is easily deformed by the EFM tip forces in contact mode, and so the position of nanoparticles cannot be guaranteed from one image to the next.

Though individual nanoparticles are unlikely to be imaged, charging over a larger scale can be investigated in order to gain a greater understanding into the role the nanoparticles play in the charging experiments performed by Ouyang *et al*. [9-10] with an investigation conducted into the EFM responses of the same polymer films used in memory devices, but without top metal electrodes, as illustrated in Figure 5.12.

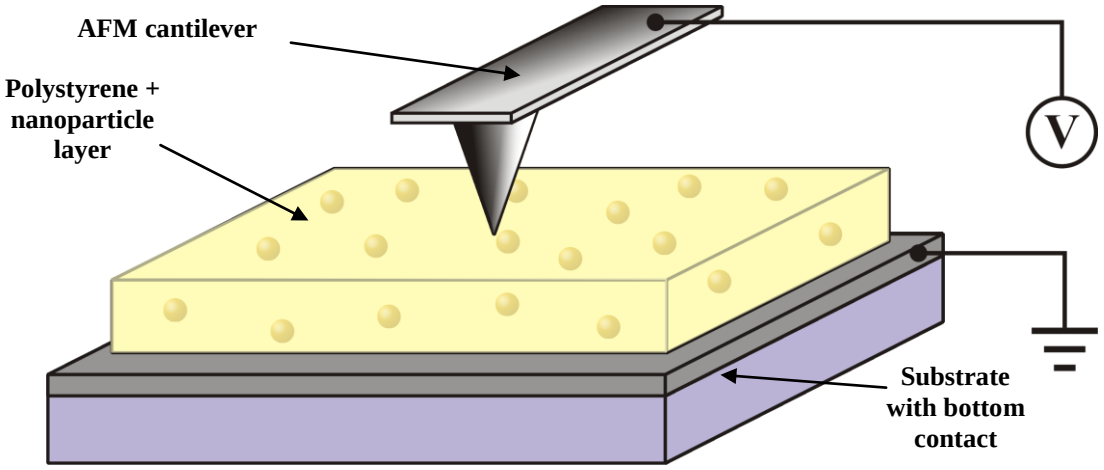


Figure 5.12 Experimental setup for Electrostatic Force Microscopy measurements.

The theory behind these experiments is that the EFM probe is in effect acting as the top contact of the device, so if *write* and *erase* voltages are applied to the probe while it is scanning across the polymer film, the nanoparticles will be charged in the same way that they would be in a normal PMD. If the nanoparticles are being charged and retaining their charge, then it will be possible to sense this charge by subsequently scanning across the polymer surface with an intermediate *read* voltage.

EFM measurements can be conducted in either contact or non-contact mode EFM, however, in order to be able to directly apply a voltage to the polymer films contact mode has to be used for both the *write* and *erase* scans. Due to this requirement, and also in order to minimise the time taken between performing the *write*, *erase* and *read* scans, the *read* scans were also performed in contact mode.

Unless specifically stated otherwise, in all EFM experiments Type-II gold nanoparticles were used. The polystyrene admixture was prepared with gold nanoparticle and 8HQ concentrations at 4 $mg \cdot ml^{-1}$ and polystyrene at 25 $mg \cdot ml^{-1}$ (referred to as PS+NP+8HQ film), to replicate as closely as possible the conditions used in [9]. Samples were also prepared with only the polystyrene layer present in order to be able to study the different responses and be able to clarify the roles the nanoparticles and 8HQ play. For all samples tested the same instrument settings were used, e.g. applied voltages and signal gain, so it is possible to directly compare the amplitude of the EFM signals for different samples.

Initial experiments were conducted on PS+NP+8HQ films, with the EFM probe biasing a square area of the polymer layer. The square was divided into two rectangles from top to bottom, with bias voltages of -10 V and +10 V being used respectively in each of the rectangles, corresponding to the *erase* and *write* voltages. Figure 5.13(a) and (b) show the

EFM phase image and topography respectively, of a subsequent larger scan over the area taken at a *read* voltage of +4 V.

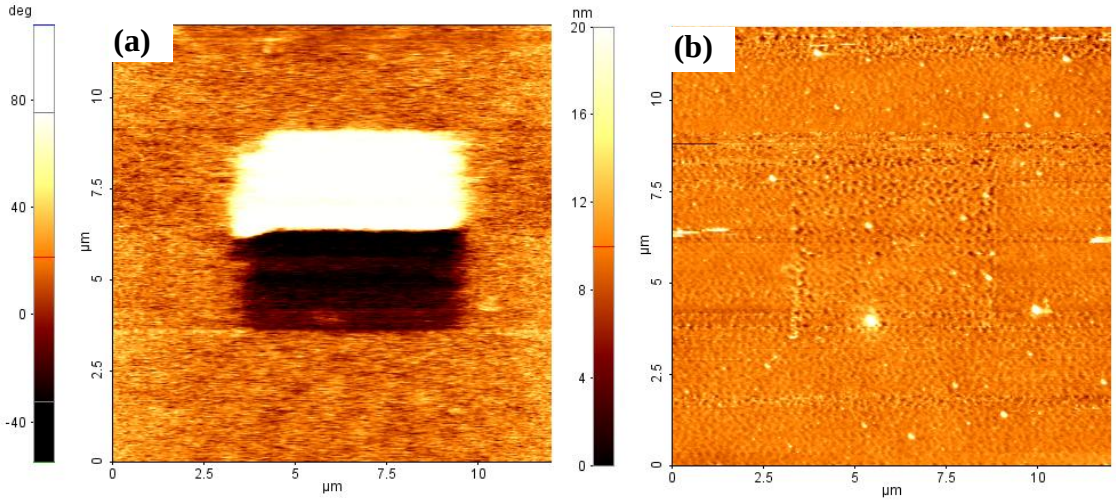


Figure 5.13(a) EFM phase response of a pre-biased area of the PS+NP+8HQ film. (b) Corresponding topography image.

It is quite clear from the EFM image that the PS+NP+8HQ film has been charged by the probe, with three distinct areas corresponding to positive, negative and unbiased regions of the film. From the topography image it is evident that there is also some damage to the PS+NP+8HQ film due to the probe being in contact mode. The possibility that any of the topographical features could be influencing the EFM signal is ruled out though, as the PS+NP+8HQ film also contains defects, which can clearly be seen in Figure 5.13(b), many of which are much larger in size than the damage caused by the EFM probe and there is no evidence that there is an EFM response from these defects.

In order to investigate the rewritable nature of the films, and ensure that the nanoparticle loaded films could be both charged and discharged, the second set of experiments consisted of biasing a square of the PS+NP+8HQ film with +10 V, then biasing a second smaller overlapping square with -10 V. The results of a subsequent scan over the area at a *read* voltage of 4 V is shown in Figure 5.14(a) and (b).

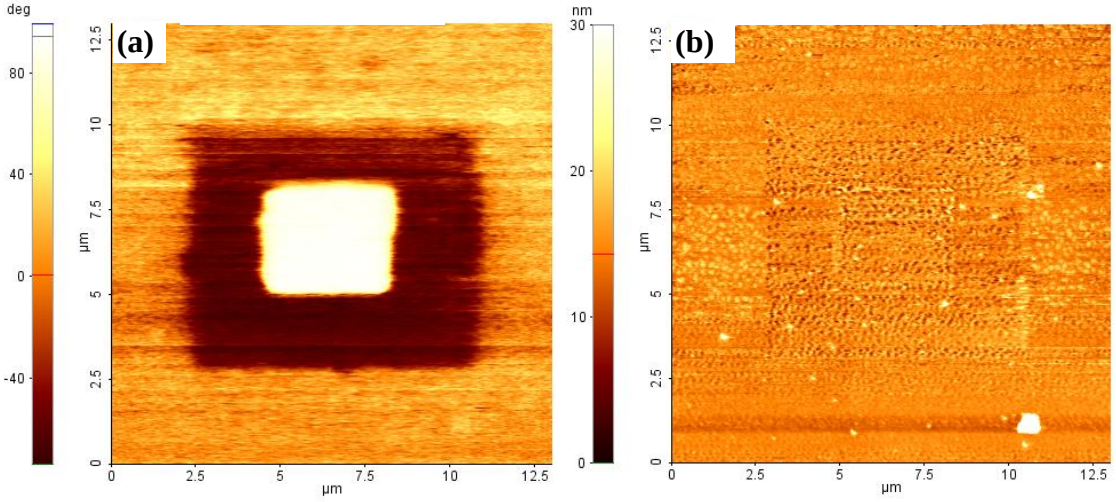


Figure 5.14(a) EFM phase response showing the rewritable charge storage of the PS+NP+8HQ film. (b) Corresponding topography image.

This clearly demonstrates that once the PS+NP+8HQ film has been positively charged it is possible to negatively charge it, as would need to be the case in a rewritable PMD.

For both of these experiments scans were also taken of the sample in succession, to gain an understanding of the length of time that the charge was retained. The EFM phase signals taken after 10, 20 and 30 minutes are shown in Figure 5.15(a), (b) and (c) respectively.

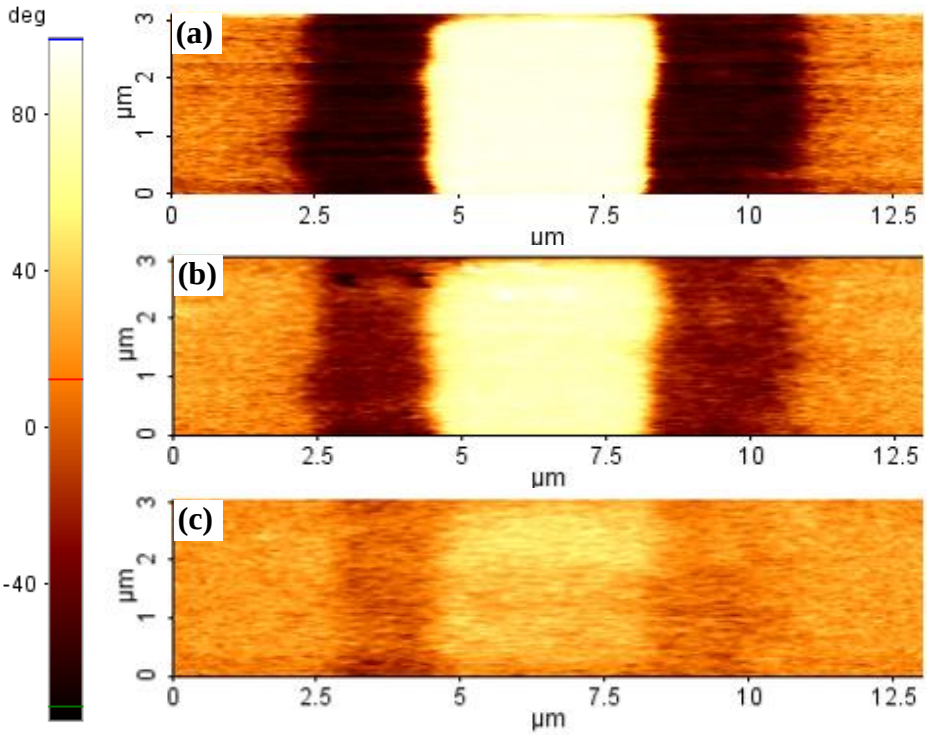


Figure 5.15 Successive EFM phase images showing the degradation of the charge response with PS+NP+8HQ films after: (a) 10 minutes, (b) 20 minutes and (c) 30 minutes.

From these images the EFM response showed no discernable difference for scans taken over 30 minutes after the area had been charged.

As previously mentioned, samples were also prepared without nanoparticles or 8HQ in the polystyrene layer, in order to make comparisons and be able to discover the exact role of the nanoparticles in the EFM signals from the films. A repeat of the same experiments conducted on the PS+NP+8HQ films showed that, in fact, an almost identical response could be measured from the films containing only polystyrene. Figure 5.16(a) and (b) show the results from a positive and negative charging of the polystyrene films and rewriting the films respectively.

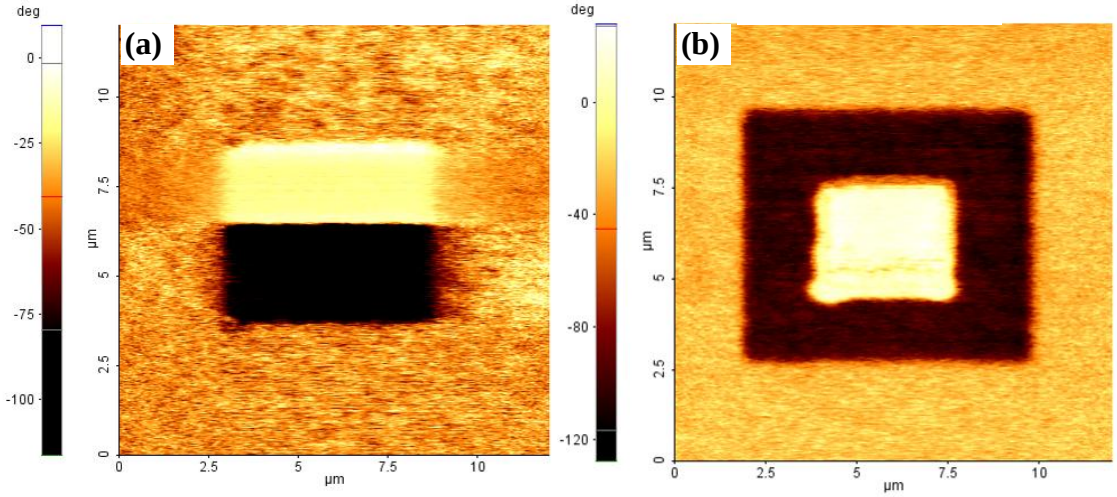


Figure 5.16(a) EFM phase response of the PS film to positive and negative biases. (b) EFM response to rewriting a portion of the PS film.

By comparing the magnitudes of the EFM signals between the polystyrene only films and the PS+NP+8HQ films it was found that the phase response was slightly diminished for the polystyrene films (125 degree difference between positive and negative areas for the polystyrene films, versus 160 degree difference for the PS+NP+8HQ films), however, the amplitude of the EFM response was comparable with ~1.2 V signal being measured from each. This indicates that the amount of charge stored by both films is of similar magnitudes and hence the charging responses of the PS+NP+8HQ films cannot solely be attributed to the presence of nanoparticles.

Successive scans were also taken of the polystyrene films, with scans after 10, 20 and 30 minutes shown in Figure 5.17(a), (b) and (c) respectively.

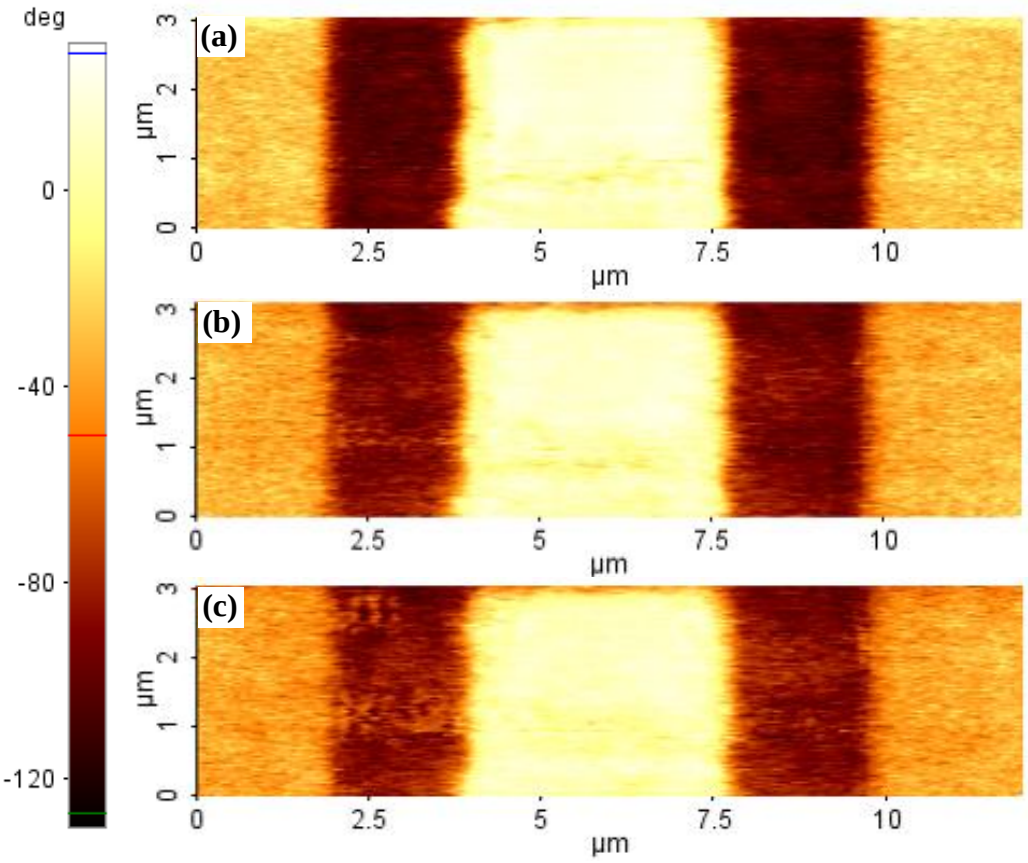


Figure 5.17 Successive EFM phase images showing the degradation of the charge response on polystyrene films after: (a) 10 minutes, (b) 20 minutes and (c) 30 minutes.

These show that the polystyrene films actually discharged at a slower rate than the PS+NP+8HQ films, with discernable differences in the charged areas being retained in excess of 30 minutes. This actually suggests that the presence of nanoparticles in the polystyrene films has a detrimental effect on their ability to retain charge. It is postulated that by introducing the nanoparticles, effectively a large concentration of conducting particles are introduced, which dissipate the stored charge. This is supported by the EFM images for the two films, where it is found that the polystyrene films show much sharper EFM features, suggesting that the charge is more effectively confined to the initially charged areas.

These experiments provide clear experimental evidence that the results of the EFM measurements made by Ouyang *et al*. [9-10] cannot be used as a claim for proof that there is a charge transfer between the nanoparticles and 8HQ molecules. Firstly, any charge storage contribution that may be present from the nanoparticles is also accompanied by a contribution from charges retained at the surface of polymer layers, which makes the charging from the nanoparticles impossible to distinguish from the background charging. Secondly, the charging that has been demonstrated here and by others [144-145] [146-147]

does not require the charge donating species (8HQ) to be present, with the charging electrons (or holes) being provided by the EFM tip or substrate. Therefore it is impossible to conclude that charge transfer from the 8HQ to the nanoparticles is the mechanism by which the nanoparticles are being charged. In order to be able to unambiguously prove that nanoparticle charging is responsible for any measured EFM signals, any possible influences from other materials have to be eliminated, as will be demonstrated in the following sections.

5.2.4.2. EFM on Langmuir-Blodgett Gold Nanoparticle Films

In order to eliminate the role that the polystyrene can play in the EFM experiments it is necessary to remove the polystyrene from the test structures completely. To accomplish this while still maintaining a sufficiently good surface on which to perform EFM experiments it is necessary to deposit the gold nanoparticles directly onto the bottom electrode via the Langmuir Blodgett technique. Type-II gold nanoparticles were used for the EFM experiments. To give the flattest possible electrode material for the bottom contact flame annealed evaporated gold on mica has been used. This substrate material yields atomically flat terraces of gold that are approximately 300 nm in size, and overall has a lower surface roughness than vacuum evaporated gold films. AFM analysis of the substrates gave route mean square (rms) surface roughness of ~3.5 nm for evaporated gold on silicon, vs ~1.2 nm for flame annealed gold on mica. (See Appendix H for comparisons of substrate materials).

Figure 5.18(a) shows clearly the presence of the nanoparticle layer, with the line analysis showing a step height of ~4 nm, corresponding well to the expected thickness of a monolayer of nanoparticles. An EFM image of the nanoparticle monolayer is also provided in Figure 5.18(b) showing the differing signals between the substrate material and the nanoparticle monolayer.

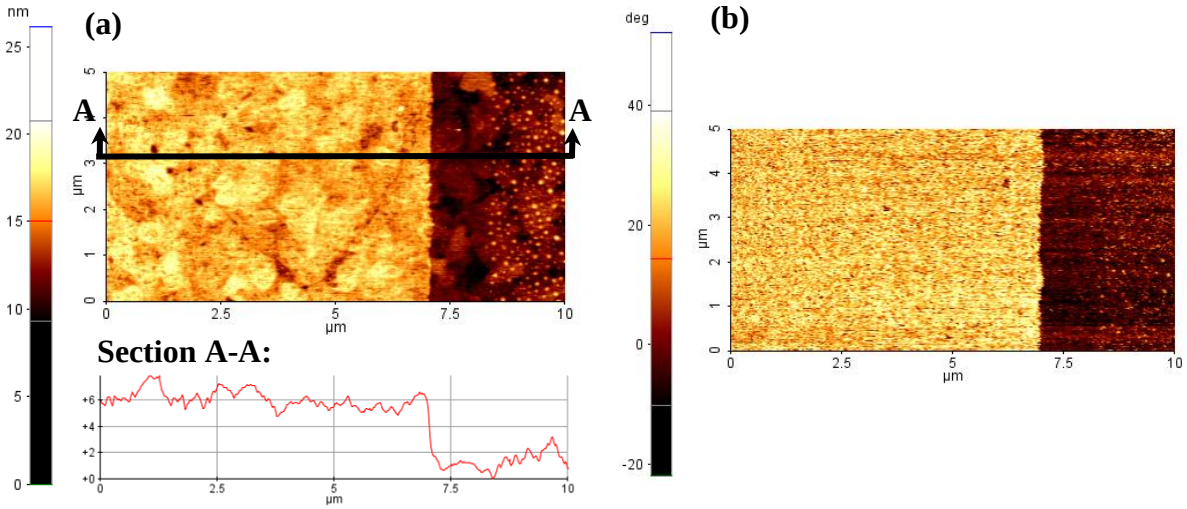


Figure 5.18(a) AFM topography image of a Langmuir-Blodgett layer of gold nanoparticles deposited on flame annealed gold on mica substrate with line profile data. (b) Corresponding EFM data showing the strong EFM contrast between the nanoparticle layer and substrate.

This is taken without any pre-biasing of the nanoparticle monolayer and serves to show that different materials can also give strong EFM signals, which will become important in the analysis of the EFM results later in this section.

As with previous experiments the charging of the nanoparticle layer has to be performed in contact mode, however, subsequent imaging of the biased areas was carried out with non-contact mode EFM to ensure imaging did not damage any areas of the substrate.

Initially rectangular areas of the substrate were biased at a positive bias of +10 V, with the subsequent *read* scan conducted at +4 V. The *read* scan EFM image and topography image can be seen in Figure 5.19(a) and (b) respectively.

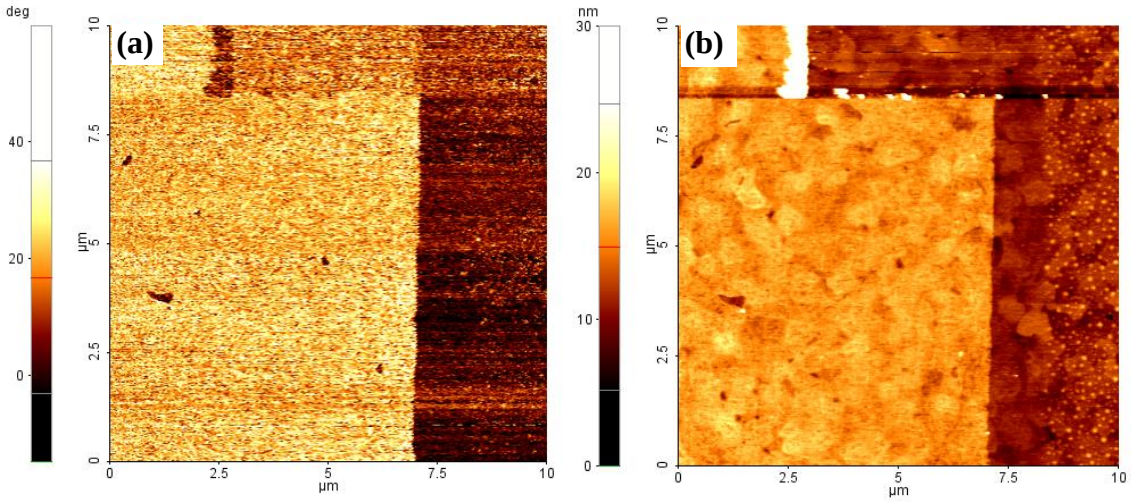


Figure 5.19 (a) EFM and (b) Topography image after a rectangular area had been scanned with the write voltage.

The rectangular scanned area can be seen at the top of the two images. It is evident that there is a slight EFM response from the area, however, if the topography image is examined it is also evident that significant damage to the nanoparticle monolayer has occurred due to the AFM probe being in contact mode. This indicates that the EFM signal is likely to be a consequence of the substrate signal rather than any influence of the nanoparticles.

Even though the forces involved in contact mode AFM are only on the order of nanonewtons, the gold nanoparticles only weakly adhere to the substrate, and so can easily be moved by the AFM probe either to the side of the scan area or onto the AFM probe itself. This interaction of AFM probe and gold nanoparticles has even been exploited by others to create nanoscale patterns by selectively removing gold nanoparticles from a substrate [143].

To ensure that the nanoparticles were not moved by the AFM probe, experiments were also conducted with the x-y scan stage of the AFM disabled. The AFM probe was then brought into contact with the nanoparticle layer with the minimum contact force needed to engage with the surface and the positive *write* voltage applied to the nanoparticles.

Figure 5.20(a) and (b) show the same area of the nanoparticle layer, both before and after the *write* voltage had been applied. The area where the AFM probe came into contact with the surface can clearly be seen in the figure as a slightly raised area, indicating that a small amount of debris was also left on the surface by the probe. This debris is likely to be nanoparticles that were present on the probe from previous scans of the substrate. The EFM response from the nanoparticles after the *write* voltage is also shown in Figure 5.20(c), showing no discernable difference between the biased and unbiased areas of the substrate with only noise being present on the EFM image.

There is the possibility that due to the size of the AFM probe (50 nm tip radius from manufacturers specifications [148]) there are only a small number of nanoparticles being charged which are below the resolution of the scan size used. This is unlikely though for two reasons: firstly EFM images with a 10 μm^2 scan size (such as Figure 5.19) gave an EFM response from pin-hole features in the nanoparticle layer with a minimum feature size of 150 nm. Therefore the smaller scan size of 4 μm^2 should be capable of responding to features that are ~60 nm in size. Secondly it is unlikely that only the nanoparticles directly under the probe would become charged, with all the nanoparticles in the vicinity of the probe expecting to be charged to some degree. For these reasons, it is unlikely that the resolution of the EFM would be too low if the nanoparticles were being charged.

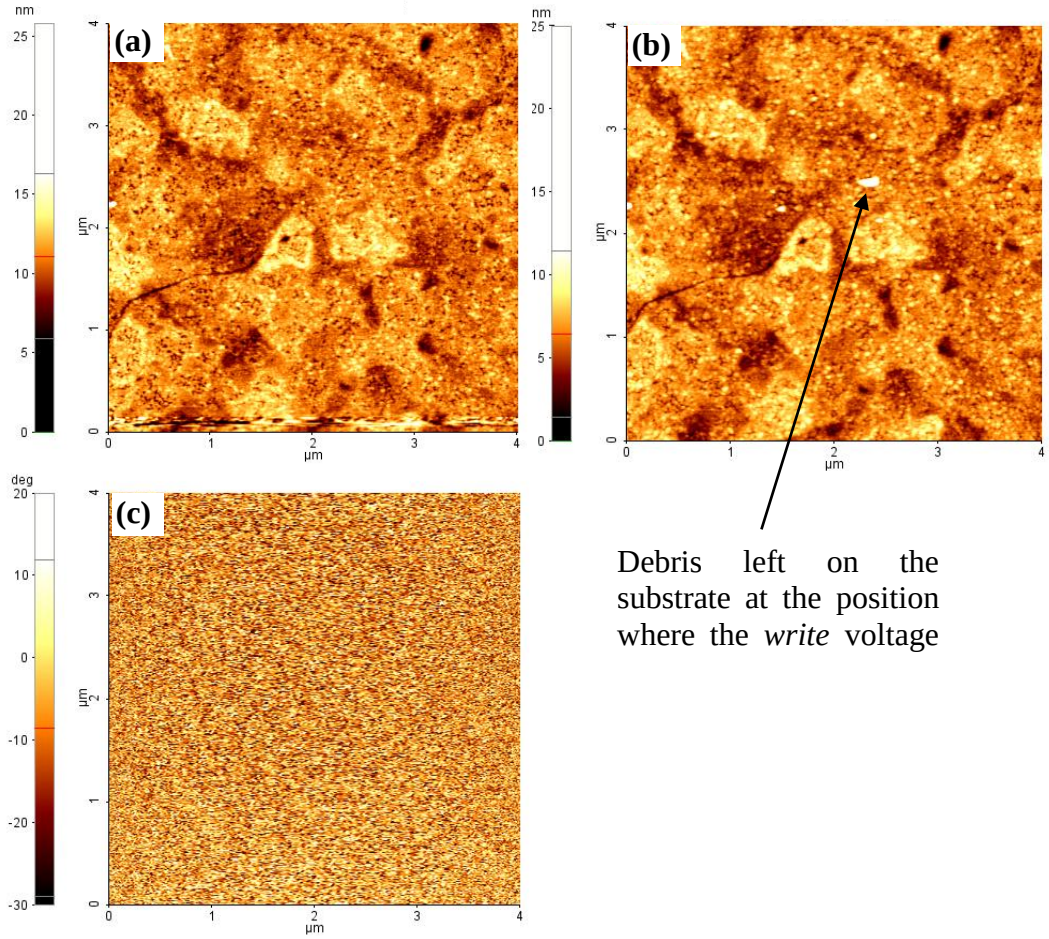


Figure 5.20(a) Topography image before application of the *write* voltage. (b) Topography image of the area after the *write* pulse, showing a small amount of debris left on the surface. (c) EFM image of the same area of the substrate.

If the debris present on the substrate in Figure 5.20(b) are nanoparticles deposited from the probe then these would certainly be expected to be charged. The fact that there is no EFM response to the nanoparticles can be attributed to one of the following:

1. The nanoparticles are not being charged.
2. The nanoparticles are not retaining their charge long enough to be imaged.

If it is assumed that the nanoparticles are being charged, then at room temperature two things will dictate the length of time it takes for the stored charge to dissipate; firstly the capacitance of the nanoparticle, C_{NP}, and secondly the tunneling resistance, R_T, of the barrier (in this case the capping ligands of the gold nanoparticle) as illustrated in Figure 5.21.

These give a time constant such that

$$\tau = R_T C_{NP} \qquad \textbf{Equation 5.7}$$

which based on the length of time taken between the *write* or *erase* scans and the *read* scan needs to be >600 seconds to maximise the chance of success.

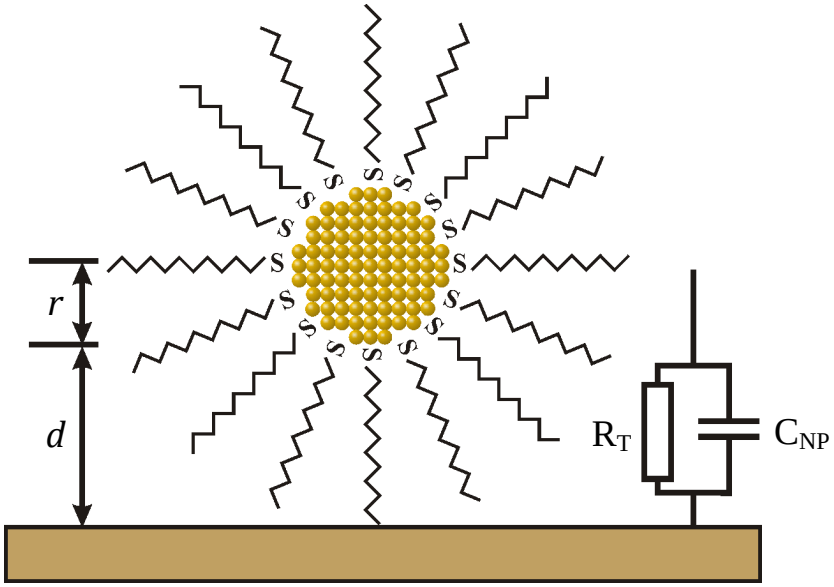


Figure 5.21 Gold nanoparticle dimensions, capacitance and tunnel resistance.

For the case of a gold nanoparticle the capacitance can once again be modelled as a conducting sphere surrounded by a finite insulating shell, using Equation 5.1. To be able to calculate a value for C_{NP} the diameter of the nanoparticles will be taken as 4.08 nm and the length of the dodecanethiol capping ligand is 1.3 nm, meaning the gold core has a diameter of 1.48 nm. (See Appendix D for specifications of Type-II gold nanoparticles). An estimate for the dielectric constant of dodecanethiol of 2.7 will also be used [149]. This gives an estimate for the capacitance of one nanoparticle to be C_{NP} ~3.5x10^{-19} F. A second way to calculate the capacitance assumes that the nanoparticle is simply a conducting sphere inside a dielectric material, as given by Equation 5.2, giving C_{NP} ~2.2x10^{-19} F. For the purposes of an estimate, a mid value of these two methods of 2.9x10^{-19} F will be used throughout the study.

In a densely packed nanoparticle monolayer, it is assumed however that an area of nanoparticles will be charged. If it is assumed that an area with a diameter of 100 nm is charged (based on the size of the EFM tip and allowing for an area around this to be charged) then the number of nanoparticles will be approximately 1000 giving a total capacitance of 2.9x10^{-16} F (based on the assumption that due to the nanoparticles being in a monolayer the capacitances would be in parallel, and so can be simply summed).

A value for R_T in alkanethiol capped gold nanoparticles has previously been reported for hexanethiol and octanethiol of 460 MΩ and 7.6 GΩ respectively [140]. As these are shorter chain lengths than the capping ligands used here, it would be expected that a higher tunnel

resistance is present in our devices. However, even if a value for R_T of 10 GΩ is assumed, this would mean that the time constant is still only 2.9 µs; many orders of magnitude too short to likely be imaged with the EFM. Two possible solutions are evident to overcome this:

1. Increase the RC time constant so the nanoparticles remain charged long enough to be imaged with EFM. This solution is implemented in §5.2.4.3 by a combination of changing the method of charging the nanoparticles, and also depositing them on insulating substrates.
2. Use instrumentation capable of measuring the charge on a faster time scale. In this case EFM imaging techniques are unsuitable and measurements have to be made electrically by measuring the charge/discharge characteristics of nanoparticle test structures with an oscilloscope, as demonstrated in §5.2.5.

5.2.4.3. EFM on Nanoparticles Deposited Between Metal Electrodes

As discussed in the previous section it is possible that the nanoparticles were being charged by the AFM tip, but the charge was dissipating before the EFM *read* image was able to be taken. This problem is likely to have been further exacerbated in the charging experiments conducted in §5.2.4.2 due to the nanoparticles being deposited on conductive substrates. The implication of this is that the only barrier to stop the gold nanoparticles discharging is the capping ligands, which are unlikely to offer a high enough resistance to keep the nanoparticles charged for any length of time.

To overcome both the problem of a conductive substrate and the need to change AFM probes before the *read* scan, structures based on depositing gold nanoparticles on an insulating substrate between metal electrodes were fabricated, with the test structure shown in Figure 5.22.

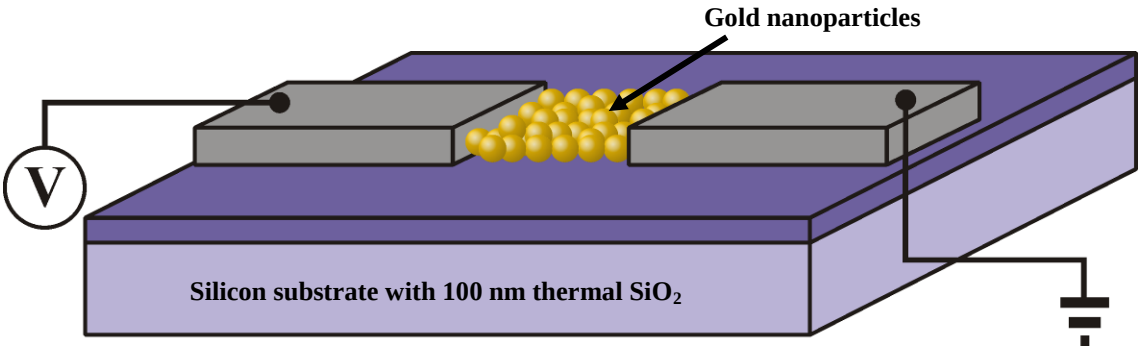


Figure 5.22 Test Structure used in modified EFM charging experiments.

In this structure aluminium electrodes ~125 nm thick were vacuum deposited onto 100 nm thermally grown SiO_2 which had been previously silanised. Gold nanoparticles were then deposited on the substrate via Langmuir-Blodgett deposition, with four layers being deposited to ensure a good coverage between the electrodes. Figure 5.23 shows an optical microscope image of the aluminium electrodes, with the gold nanoparticle layers also being visible. To further confirm the deposition of nanoparticles between the electrodes *I-V* characteristics were taken before and after the nanoparticle deposition, with an order of magnitude increase in current when nanoparticles were present.

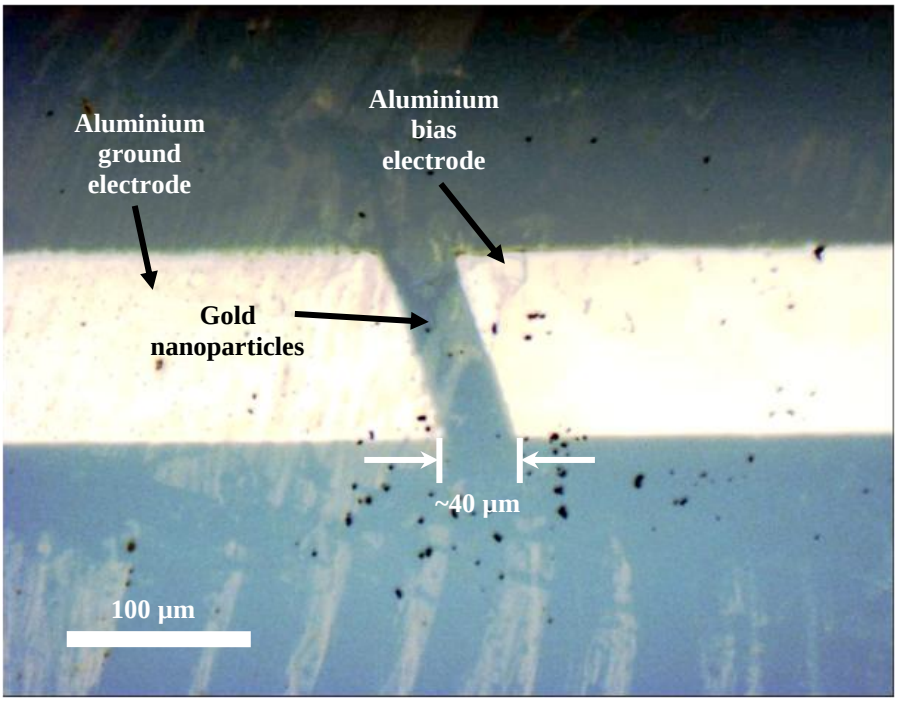


Figure 5.23 Optical image showing gold nanoparticles deposited between aluminium electrodes.

Instead of using the EFM probe for the *write* and *erase* scans, in this arrangement voltages can be applied across the nanoparticles by applying voltage biases directly to the aluminium electrodes, enabling EFM images to be taken on a continuous basis. This greatly enhances the likelihood of being able to quickly image any changes to the charge state of the nanoparticles. In Figure 5.24(a) the topography image shows the area on the substrate where the EFM charging experiments were conducted, with the smaller central portion of nanoparticles being in electrical isolation, while the other areas were all in electrical connection with the grounded electrode. It was found that having an isolated area of nanoparticles was actually critical in measuring a response via EFM. This is likely to be for several reasons. Firstly, in areas where a continuous layer of nanoparticles were connected to the electrodes there was no reference voltage present in the images, making it difficult to

obtain unambiguous EFM data. Secondly, the nanoparticles that were in electrical connection with the electrodes didn't appear to hold charge long enough for meaningful measurements to be taken, indicating that the charge could easily dissipate through the nanoparticle layers.

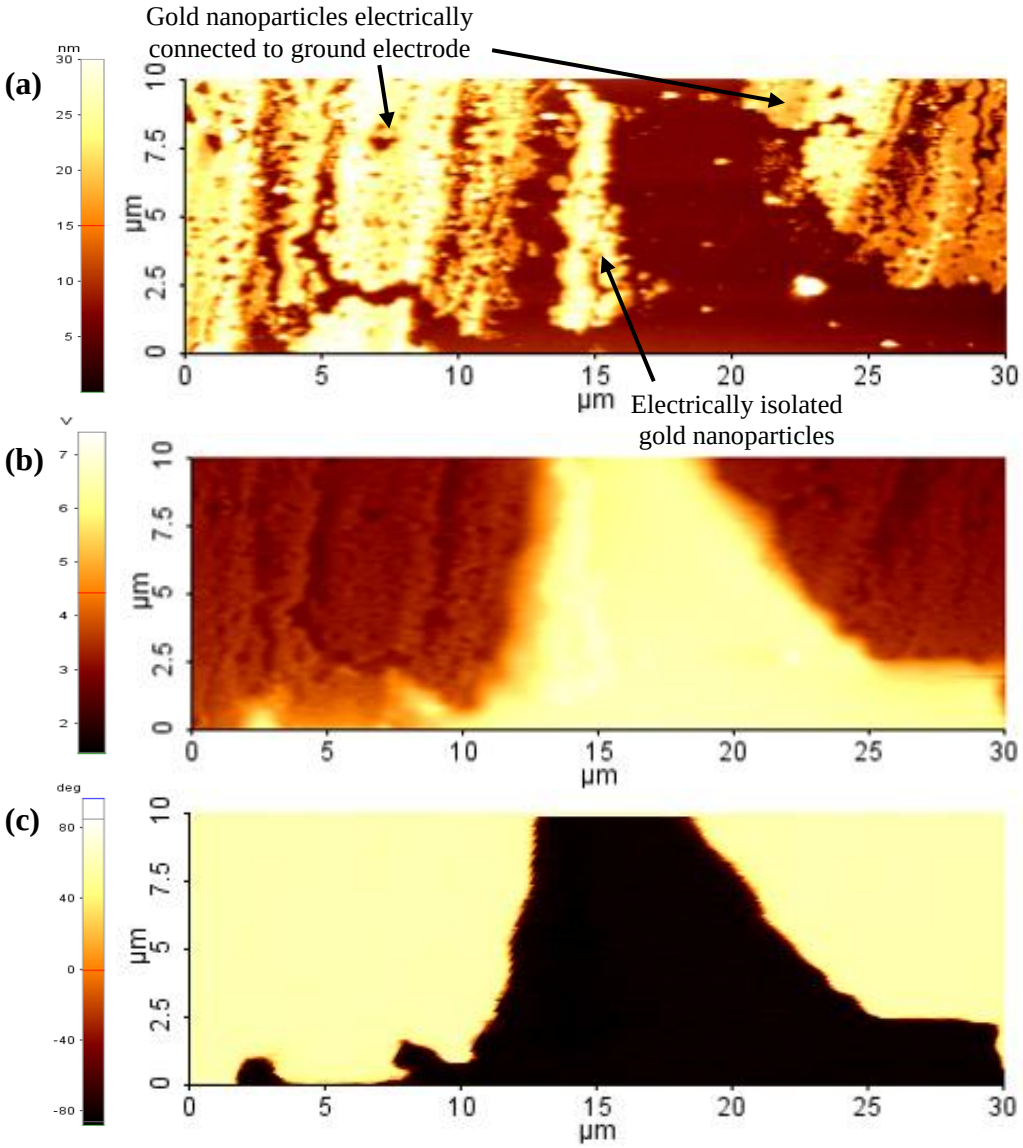


Figure 5.24(a) Topography image of the area where nanoparticle charging experiments were conducted. (b) EFM amplitude and (c) phase image when an external voltage of +10 V is applied to the bias electrode.

As the nanoparticle island was not in electrical contact with the grounded nanoparticles it allowed the contrast between charge levels of the two to be easily sensed by the EFM. Figure 5.24(b) and (c) are the amplitude and phase EFM signals respectively when a positive bias of 10 V was applied to the bias electrode, which shows conclusively that the two areas of nanoparticles are not electrically connected with each other. By applying ±10 V to the bias electrode it was found to be possible to charge the central area of nanoparticles, with a clear

difference in the EFM response of the area when it was *read* with an EFM tip bias of 3 V, as shown in Figure 5.25(b) and (c).

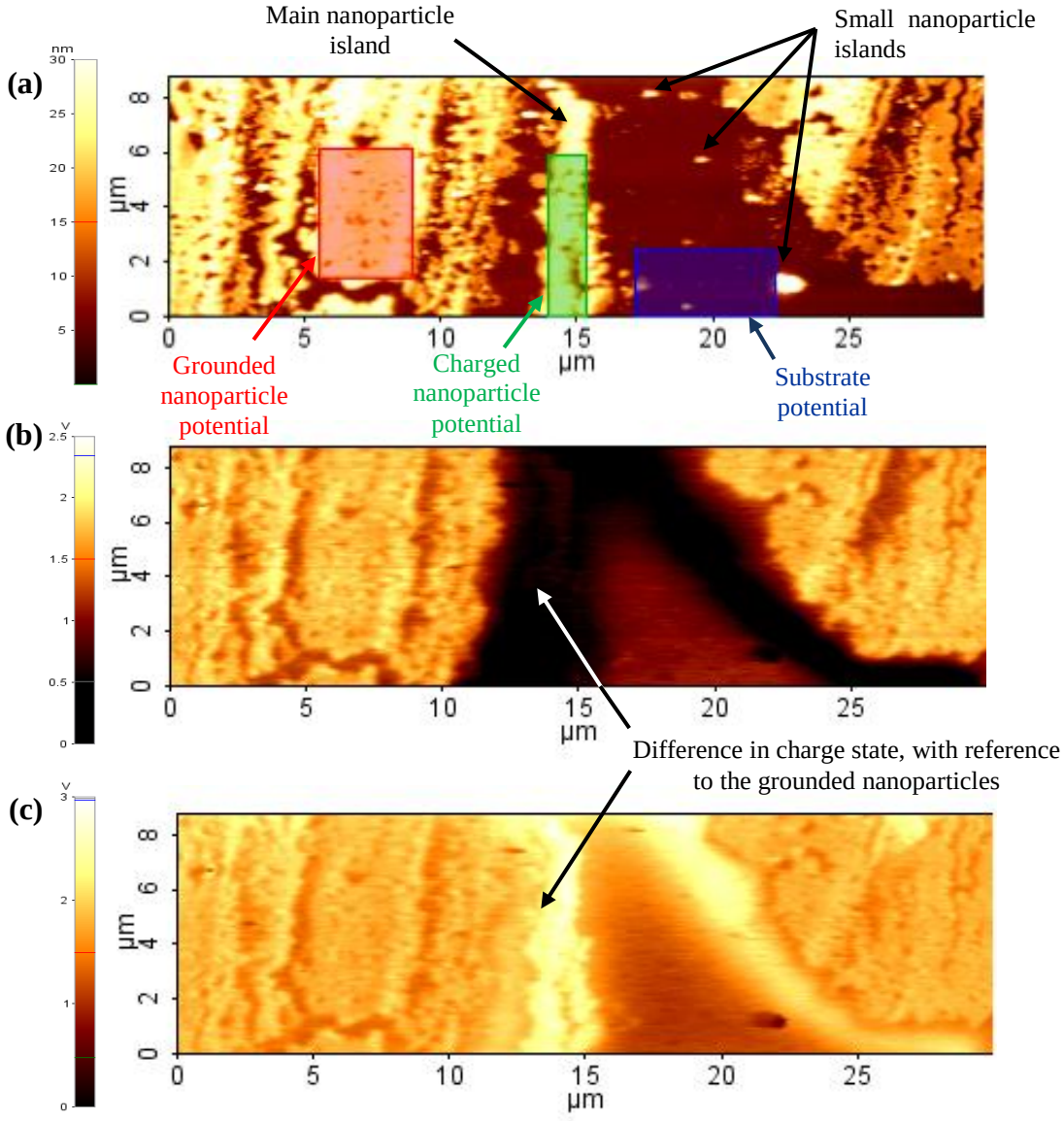


Figure 5.25(a) Areas where the potential information was measured for the grounded nanoparticles (red), charged nanoparticles (green) and substrate (blue). First *read* scan after a bias of (b) +10 V and (c) -10 V.

Repeated scans at the *read* voltage were then taken in order to highlight the slow discharge of the nanoparticles, with the charge levels returning to their pre-charged state after approximately 20 minutes. (The full sequence of *read* scans is included in Appendix I.)

Potentials for the grounded nanoparticles, charged nanoparticles and the substrate were measured as a function of time. The positions where the three values were measured from is shown as the coloured rectangles in Figure 5.25(a). Identical measurement conditions were

also maintained throughout all the scans (voltage bias, voltage gain etc.), so that it is possible to make a direct comparison between the magnitudes of the measured potentials (and hence the magnitude of the stored charge, as charge is proportional to voltage).

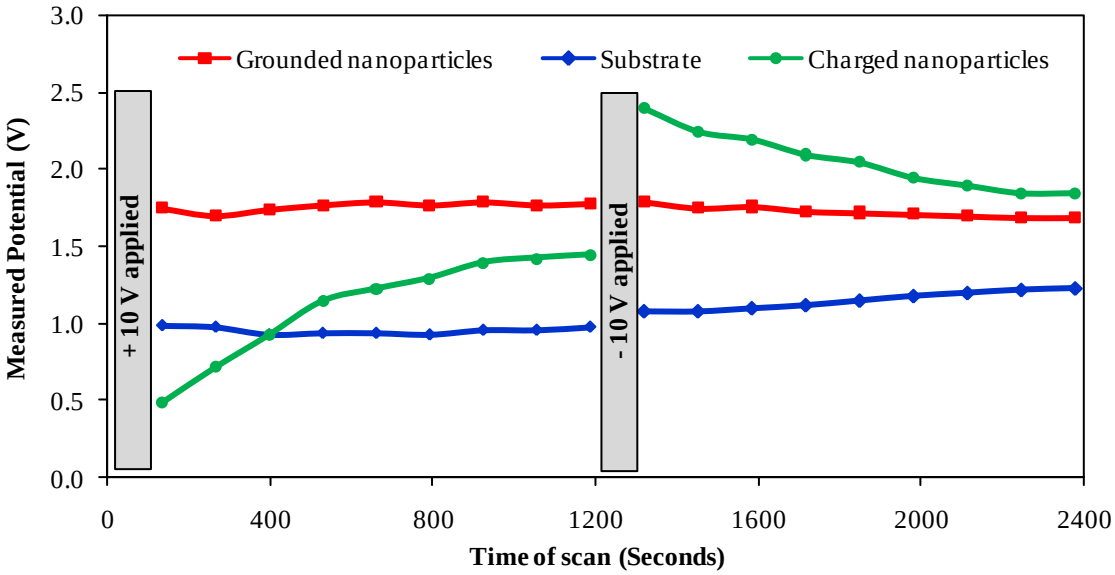


Figure 5.26 Potentials of charged nanoparticles and reference areas.

Here it is possible to see that while both the grounded nanoparticles and the substrate remain at approximately a constant potential, the nanoparticles connected to the bias electrode show a significant change in potential. As would be expected for a stored charge being dissipated, both charged nanoparticle curves show an exponential decay towards the potential of the grounded nanoparticles. It is also evident from both Figure 5.26 and the EFM images in Figure 5.25 that the grounded nanoparticles and the substrate do not measure the same potential, despite them in theory being at the same potential with no external bias applied. This is actually to be expected, as different materials will also give a different EFM response, as has previously been discussed in §5.2.4.2.

There is the possibility that the different potentials could be a result of the substrate or the electrode being charged rather than the nanoparticles. There is evidence to suggest that the substrate is following the potential of the bias electrode, as can be seen from the EFM potential in Figure 5.24(b) where the whole substrate area as well as the isolated nanoparticles show a high potential when +10 V is applied. If the substrate and the bias electrode are at the same potential then this immediately precludes the possibility of a capacitor forming between the two. If the whole substrate/electrode system is holding charge then this would be expected to discharge rapidly as it is only discharging through the resistance of the instrumentation. Any isolated charged nanoparticles on the SiO_2 either have

to discharge through the SiO_2 itself, or tunnel onto the closest neighbouring nanoparticles and then the electrodes, resulting in a much greater resistance and hence a much longer time constant. In Figure 5.25(b) and (c) the substrate also seems to give an EFM response around the perimeter, near to where it meets the grounded nanoparticles. The data is rather ambiguous as to whether this is a true response from the substrate, or whether it is simply an artefact of the EFM images. If this is a true response, then it is only evident for the initial few minutes of the *read* scans, giving a much faster discharge rate than that of the charged nanoparticles. For this reason it is possible to rule out the possibility of the substrate holding charge as being responsible for the EFM response of the nanoparticle island.

By setting the grounded nanoparticle potential to zero volts and using this as a reference point for the magnitude of the potentials of the charged nanoparticles, the discharge curves for both charge states can be plotted, with the results shown in Figure 5.27.

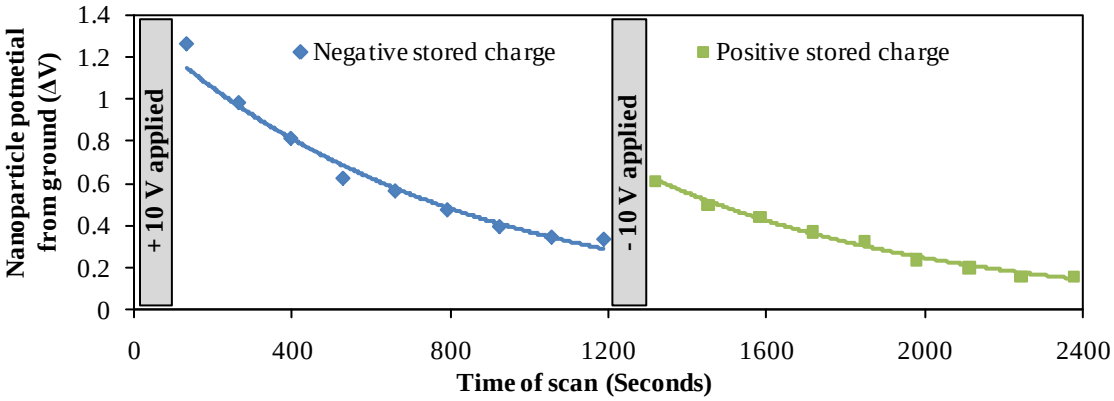


Figure 5.27 Discharge curves for the gold nanoparticles after ±10 V biases with exponentially decaying best fit lines.

Two interesting features immediately become evident; firstly it is seen from Figure 5.26 that a positive bias voltage leads to a negative stored charge and vice versa (i.e. electrons are being stored under a positive bias). This would indicate that under positive bias electrons are being injected from the grounded nanoparticle layer and becoming trapped on the nanoparticle island due to the SiO_2. From the topography images of the area it is not possible to get accurate estimates for the distance from the grounded nanoparticles to the isolated island, but especially towards the top of the island the distances are small enough to be below the resolution of the topography image (<50 nm) and could be considerably less. With charging voltages of ±10 V used this equates to electric field strengths of >2.0 $MV \cdot cm^{-1}$ which may be great enough to allow tunneling of electrons. Secondly the nanoparticles show a higher initial potential after a positive bias has been applied, i.e. they store a greater

negative charge relative to the grounded nanoparticles than a positive charge. Gold nanoparticles have been shown to be both donors and acceptors of electrons depending upon the application where they are being used [90-91]. The greater negative charge stored on the nanoparticles here, suggests that the Type-II gold nanoparticles are able to accept a greater number of electrons than they can donate.

The charged nanoparticles also show good agreement with the expected exponential decay in potential as they discharge. If the theoretical equation for the discharge of a capacitor is fitted:

$$Q = CV_0 e^{-t/RC} \qquad \textbf{Equation 5.8}$$

Then it is found that for negative stored charge:

$$Q_N = 1.36Ce^{-t/771}$$

and for positive stored charge:

$$Q_P = 0.74Ce^{-t/735}$$

This gives RC time constants of 771 and 735 seconds for negative and positive charge respectively, which are both in good agreement suggesting the origin of the charge is the same. From the topography images of the nanoparticle island it is possible to get an estimate for the volume enclosed, and hence the total capacitance, based on a simple summation of nanoparticle capacitances. This method gives a total capacitance of 2.32 pF, from which the estimated value of the discharging resistance is ~3.24×10^{14} Ω. By estimating the resistance of the SiO_2 insulator to be ~5.6×10^{15} Ω this value of discharge resistance is possible for these devices. (See Appendix F1 for calculation). As previously discussed from the polarity of the stored charge compared with the charging voltage it is likely that charging/discharging is taking place through tunneling from the grounded nanoparticles. This is also corroborated by the fact that there are smaller nanoparticle islands present in Figure 5.25(a) which show no evidence of charging due to their further distance from the grounded nanoparticles.

5.2.5. Oscilloscope Measurements of Gold Nanoparticle Charging

An alternative approach to demonstrate the charging of the gold nanoparticles is to make use of equipment capable of measuring the charging and discharging of the nanoparticles at significantly faster speeds. This necessitates a move away from EFM based measurements to one based around the electrical response of the nanoparticles to a voltage pulse, measured via an 600Mhz LeCroy WaveRunner 64Xi oscilloscope. The basic circuit used in these

experiments consists of a simple series resistor capacitor circuit, as shown in Figure 5.28. The device under test (DUT) is connected to the circuit via a probe station.

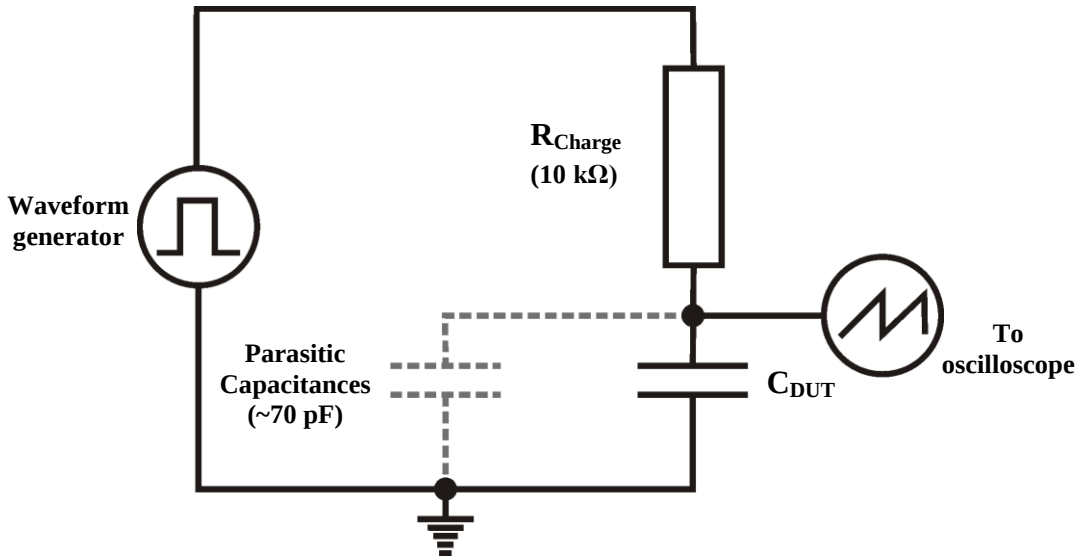


Figure 5.28 Resistor, capacitor test circuit used for nanoparticle charging.

With this circuit it was found that there were some parasitic capacitances present even when the DUT was not connected (i.e. this connection was an open circuit). However, only the changes in capacitance due to introducing the nanoparticles are of interest, hence this parasitic capacitance does not pose a problem. By replacing the DUT with known capacitances it was confirmed that the parasitic capacitances were in parallel with the DUT, meaning that the total capacitance in the circuit is simply the sum of the parasitic capacitance and C_{DUT}. Measurements on various parts of the circuit resulted in the following estimates being made:

- Total parasitic capacitance < 70 pF
- Capacitance due to probe station ~30 pF
- Capacitance due to oscilloscope inputs/cables ~40 pF

Initial devices tested consisted of the same geometry as those used for the EFM measurements in §5.2.4.3, i.e. 100 µm wide electrodes separated by a 40 µm gap where nanoparticles are deposited. In order to minimise the capacitance of the metal tracks in these experiments the break junctions were fabricated on insulating substrates of sapphire, so all charging had to be a result of the electrode potential, rather than any substrate potential, as was likely the case in the EFM experiments in §5.2.4.3. Capacitance measurements for these devices are shown in Figure 5.29, with the three capacitance values corresponding to the open circuit capacitance (i.e. total parasitic capacitance), the capacitance of the pristine

junctions before the deposition of nanoparticles, and the capacitance of the junctions with nanoparticles deposited.

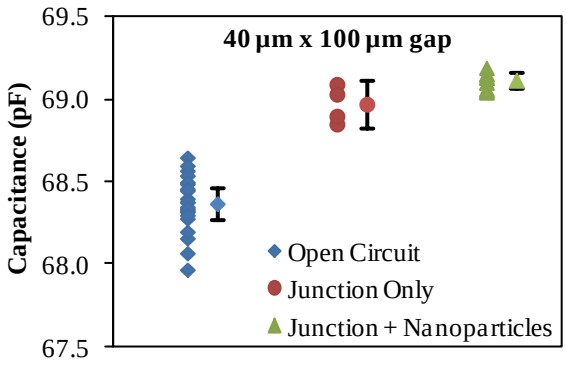


Figure 5.29 Capacitances of 40 µm x 100 µm gap, with averages and 99% confidence interval shown next to the data points.

This gives a value of the parasitic capacitance in the range (68.27, 68.46) pF based on a 99% confidence interval, and likewise a capacitance range of (68.82, 69.11) pF for the empty junctions and (69.07, 69.16) pF for the junctions with nanoparticles. This equates to approximately 0.60 pF capacitance that can be attributed to the junctions themselves and ~0.14 pF that can be attributed to the nanoparticles. Considering the overlap of the confidence interval ranges and the small increases in capacitance it is not possible to conclude with certainty that these increases are due to the nanoparticles. In this case, the conclusion is that in this experimental configuration there is no evidence of the nanoparticles being charged.

A possible explanation could be offered by considering that so far single monolayers of nanoparticles have been studied, where the capacitances have been modelled as being in parallel. In this situation the electrodes will actually contain a volume of nanoparticles between them, in essence giving a large array of series and parallel capacitors and resistors. The analysis of this system would likely be a huge undertaking and is outside the scope of this project, but the overall capacitance would certainly be orders of magnitude smaller than the simple sum of the individual nanoparticle capacitances. As a solution to this problem, devices were fabricated using break junctions as the electrodes, with the aim of reducing the amount of nanoparticles in series. Electrode widths of both 100 µm and 250 µm were evaporated as the basis for the junctions, with the same fabrication procedure as that described in §5.3 used. In theory the capacitance of the gold electrodes themselves should increase between the 100 µm and 250 µm widths, but as the break junctions should be of similar dimensions, the increase in capacitance due to the nanoparticles should remain

constant. The results of these experiments are shown in Figure 5.30, with a summary of the data presented in Table 5.1.

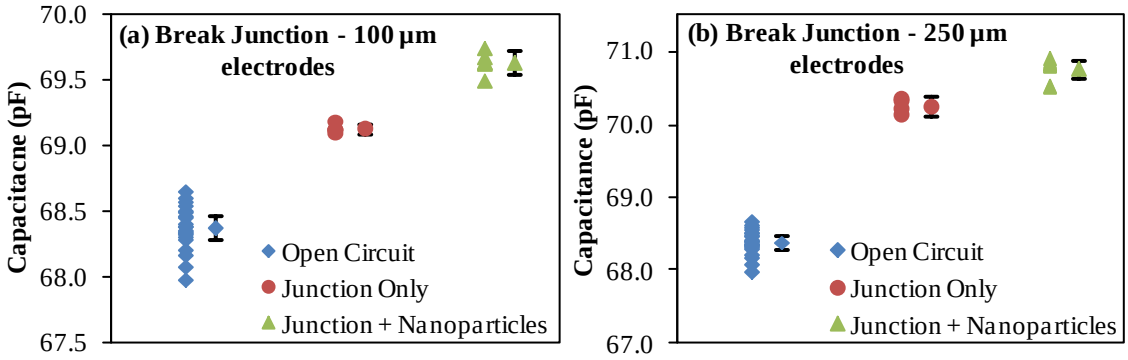


Figure 5.30 Capacitances of (a) Break junction fabricated from 100 µm wide lines and (b) Break junction with 250 µm wide lines. Averages and 99% confidence interval shown next to the data points.

Table 5.1. Summary of capacitance ranges based on 99% confidence interval for gold nanoparticle filled break junctions. All measurements in pF.

Device	Open circuit (parasitic)	Electrodes + parasitic	Nanoparticles + electrodes + parasitic	Capacitance attributed to electrodes	Capacitance attributed to nanoparticles
100 µm wide electrodes	(68.27, 68.46) Average = 68.37	(69.09, 69.16) Average = 69.12	(69.54, 69.72) Average = 69.63	0.76	0.51
250 µm wide electrodes	(68.27, 68.46) Average = 68.37	(70.11, 70.38) Average = 70.25	(70.63, 70.88) Average = 70.75	1.88	0.51

These values do follow the predicted trend of the junction capacitance increasing, while the nanoparticle capacitance remains constant. To confirm these capacitance values the expected capacitances of the electrodes can be calculated from Equation 4.7, by assuming that the electrode capacitance is a result of the biased portion of the electrode forming a capacitor with the grounded probe station chuck, separated from the electrode by the thickness of the glass substrate slide (~200 µm). Using a dielectric constant of 6.7 [150] would give capacitances of ~0.8 pF and ~1.3 pF for the 100 µm and 250 µm electrodes respectively (see Appendix F2), which are in reasonable agreement with the measured values.

The increase in capacitance due to the nanoparticles is more difficult to confirm. The whole area between the break junction is estimated to be approximately 5 µm length x 30 nm height x 30 nm wide, and is assumed to be filled with nanoparticles, resulting in an array of nanoparticles as described previously. However, even if it is assumed the total capacitance is a sum of the individual nanoparticles' capacitances (which is likely to be a gross

overestimate) then this would only be expected to contribute ~0.04 pF. (see Appendix F3). If the reverse of this is considered, it is possible to calculate that the area of nanoparticles in parallel required to give ~0.5 pF capacitance would be ~20 μm^2. As the nanoparticles are drop cast onto, and between the electrodes, a significant portion of the electrode itself is also covered in nanoparticles. It is possible that these nanoparticles are also being charged and contributing to the overall capacitance. A second possibility is that the addition of the nanoparticles is simply increasing the effective electrode area. To provide the extra 0.5 pF of capacitance the electrode area would only need to the increased by ~1.75 mm^2, an area that could easily be provided by the drop cast nanoparticles.

Circuit simulations were performed using the measured capacitances from the 250 µm electrodes, first, to confirm the initial assumptions that the parasitic, electrode and nanoparticle capacitances are in parallel with each other, and secondly to gain an insight into the role the nanoparticles are playing in altering the capacitance. The simulated response to a 10 V step impulse with the parasitic capacitance is shown in Figure 5.31(a) while the full circuit response is shown in Figure 5.31(b).

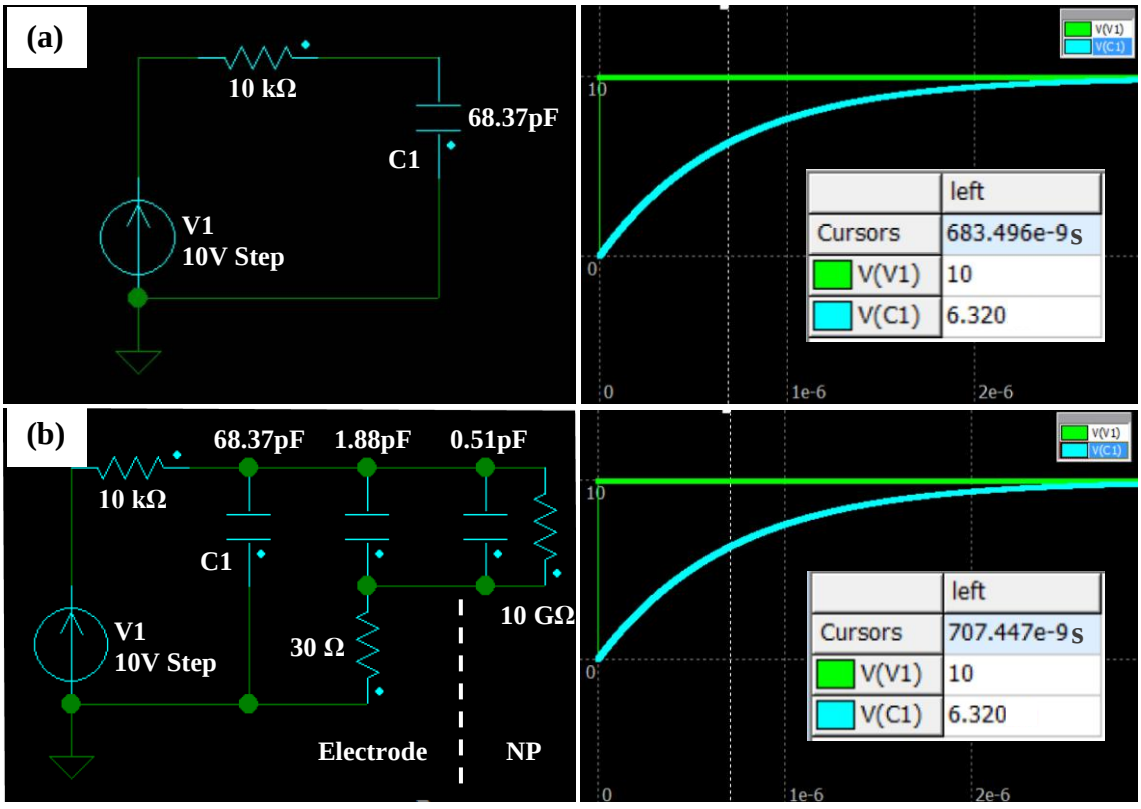


Figure 5.31 Circuit and simulated response to a 10V step input for (a) Parasitic capacitance and (b) Parasitic, electrode and nanoparticle capacitance in parallel.

For the full circuit response an extra 30 Ω of resistance is calculated to be present due to the resistance of the electrodes, while a tunnel resistance of 10 GΩ was assumed for the nanoparticles. However, provided the electrode resistance is low, and the tunnel resistance is much greater than the charging resistance, the circuit performance can be considered independent of these values. The response of the real circuit is in excellent agreement with the simulation, with a simulated RC time constant of 707.4 ns, versus an average experimental time constant of 707.5 ns. It was also found that there was no drop in voltage measured across C1 when the electrode and nanoparticles were present in the circuit, confirming that the tunnel resistance is much greater than the charging resistance, and that the simulated circuit is a good model of the real circuit. This also confirms that the extra capacitance that is due to the nanoparticles is in parallel with the electrode capacitance, which suggests that this extra capacitance is a result of the electrode area being increased, rather than the charging of the nanoparticles. Therefore with these electrode configurations it is also not possible to attribute the measured increase in capacitance to the charging of gold nanoparticles.

5.2.6. Gold Nanoparticle Charging in MIS Capacitors

The metal-insulator-semiconductor capacitor structure (which was extensively studied in §4.5 when trapped charges in polystyrene films were being investigated) is a device very sensitive to small levels of trapped charge. Using similar capacitance-voltage techniques as those applied to the study of the polystyrene films it is possible to measure charge densities as low as 10^9 cm^{-2} [128]. By selectively introducing trapped charge into MIS capacitor structures in the form of gold nanoparticles it is possible to demonstrate their charging and discharging.

Following the theory discussed previously, to have the most effect on flatband voltages of an MIS capacitor the trapped charges and so the nanoparticle layer must be as close as possible to the semiconductor boundary. However, there is also the requirement that the gold nanoparticles should maintain their charge, and so a thin insulating layer must be present between themselves and the semiconductor. MIS capacitors with the structure shown in Figure 5.32 were fabricated for studying the charging properties of the gold nanoparticles.

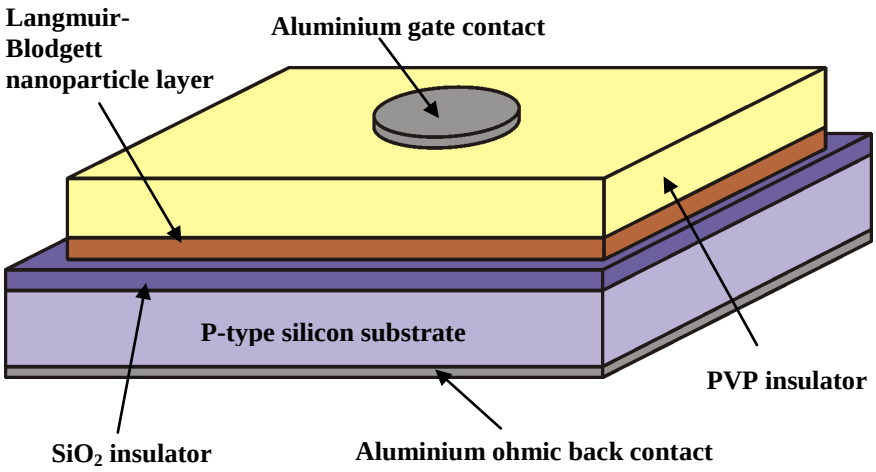


Figure 5.32 MIS capacitor structure used for studying gold nanoparticle charging.

Conventional thermally grown silicon dioxide films can be difficult to grow at thicknesses below 10 nm due to their different growth kinetics at thicknesses below approximately 20 nm [151]. It is however possible to chemically grow thin films of SiO_2 by exposing the clean silicon to nitric acid (HNO_3) [152-153]. Using this method high quality thin SiO_2 layers between 1.5 – 3.0 nm can be reliably grown.

Devices were fabricated by leaving clean p-type silicon in nitric acid for 1 hour at 60 °C then leaving for ~12 hours at room temperature. The resulting oxide proved to be too thin to reliably measure with an ellipsometer, though changes to the surface could be confirmed from contact angle measurements, with measured contact angles of 44° and 26° measured before and after nitric acid treatment respectively (see Appendix G). This indicates that the surface has become more hydrophilic, as would be expected for a SiO_2 surface. In order to deposit gold nanoparticles on the SiO_2 films they were then dipped in silanisation solution (~5% dimethyldichlorosilane in heptanes) for 15 minutes, which once again rendered the SiO_2 hydrophobic, with a contact angle of 95°. The Langmuir-Blodgett technique was then used to deposit uniform layers of Type-II gold nanoparticles. In order to investigate the effects of different amounts of nanoparticles on the amount of trapped charged present in the MIS capacitors, devices using either 2-dips, 4-dips, 8-dips or 10-dips (with one dip being defined as one downward and one upward stroke) were fabricated. As deposition was found to occur only on the downward stroke these devices are assumed to have the same number of monolayers as dips, and hence will be referred to as 2L, 4L, 8L and 10L devices. A 50 nm insulating layer of poly-4-vinylphenol (PVP) was then evaporated on top of the nanoparticle layer followed by evaporation of 250 µm diameter, 100 nm thick aluminium gate electrodes.

The spin-coating technique was not used here for the insulating layer due to the low adhesion of the nanoparticles to the SiO_2. If spin-coating was used it is likely that a significant amount of the nanoparticles would be removed with the solution. PVP was chosen as the insulating layer over the previously used polystyrene layers due to its much lower molecular weight (~25,000 for PVP versus ~280,000 for PS) which meant the success of vacuum evaporation of the PVP without significant degradation of the polymer chains was more likely [154].

The theory behind how the flatband voltage of the MIS capacitors will be altered by the trapped charges stored on the nanoparticles can be compared to the theoretical relationships established in §4.4 with the trapped charge due to the nanoparticles, Q_{np} being calculated from:

$$Q_{np} = \Delta V_{FB} \times C_{ins} \qquad \textbf{Equation 5.9}$$

To ensure that reliable *C-V* measurements were obtained the leakage currents passing through the capacitors were determined, with typical results shown in Figure 5.33.

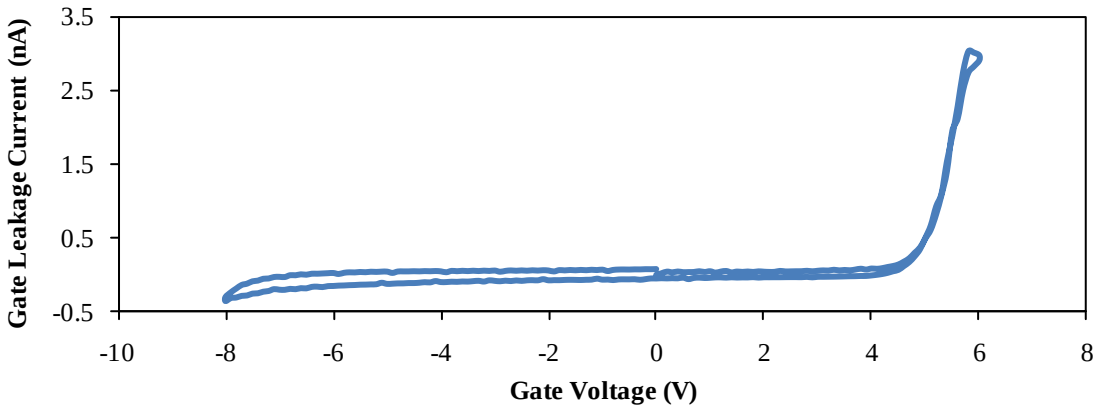


Figure 5.33 Current-voltage characteristics of a typical nanoparticle MIS capacitor.

For all the capacitors measured, the maximum leakage current (at +6 V gate voltage) was 6 nA with an average leakage current of 3 nA, demonstrating that they can reliably be operated between scanning voltages of -8 V to +6 V without risk of damage to the devices. For all *C-V* characteristics measured a voltage scan rate of 0.5 $V \cdot s^{-1}$ was used.

As can be seen from Figure 5.34, which shows a typical *C-V* curve for a 10L MIS capacitor, as the voltage scanning window is increased the amount of hysteresis also increases.

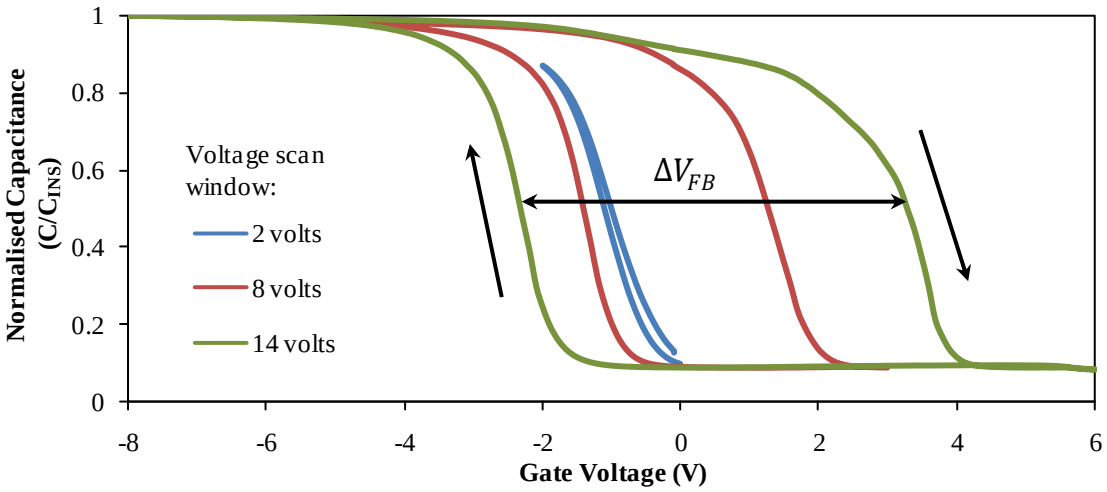


Figure 5.34 Hysteresis in the nanoparticle MIS capacitors vs. gate voltage scanning window. In all cases hysteresis was in the clockwise direction as indicated by the arrows.

If the amount of hysteresis present in these curves is examined, from Equation 5.9 and the known device geometry, the levels of trapped charge are of the order of 10^{12} cm^{-2}, so any mechanism responsible for the hysteresis has to be able to provide this magnitude of trapped charge. While the main premise of these devices is that charge trapping in the nanoparticle layer is responsible for the hysteresis in the *C-V* characteristics, there are several possible mechanisms that could result in hysteresis in the MIS capacitors:

1. Interface trapped charges in the SiO_2 insulator.
2. Insulator trapped charges in the PVP insulator.
3. Mobile trapped charges in the PVP insulator.
4. Charge trapping and de-trapping of the gold nanoparticles.

To be able to conclusively state that the hysteresis present is a result of charge trapping by the nanoparticles it is necessary to eliminate the other possible mechanisms.

As these devices have a thin layer of SiO_2 there is the possibility of the presence of interface trapped charge. Studies on SiO_2 films grown via the nitric acid solution method have previously shown that interface trapped charge density is comparable to thermally grown oxide and is likely to be in the range of approximately 10^{11} cm^{-2}, which is an order of magnitude lower than the levels of trapped charge that are necessary here [152]. Also interface trapped charge tends to produce a stretch-out effect in the *C-V* characteristics, rather than a flatband voltage shift in the whole curve. As the hysteresis effects shown in Figure 5.34 do not show any significant evidence of stretch-out, with voltage shifts remaining

largely parallel, it is possible to conclude that interface trapped charges do not play a significant role here.

In structure, polystyrene and PVP are very similar, as is evident from the chemical structures shown in Appendix D. It is likely that similar levels of insulator trapped charge and mobile trapped charge are likely to be present in the PVP insulator as were found to be present in polystyrene in §§4.5.2 – 4.5.3. Fixed insulator charge in polystyrene MIS capacitors was found to be in the order of 10^{12} cm^{-2}, however, it is not charged and discharged, so does not result in large amounts of hysteresis, merely a shift in the flatband voltage of the entire *C-V* characteristic. Therefore there is no reason to believe that fixed insulator charges will be responsible for hysteresis when PVP is used, hence this source can also be ruled out. Mobile trapped charge densities are likely to be the highest compared to the other forms of trapped charge (~$2x10^{12}$ to $3x10^{12}$ cm^{-2} if similar levels to polystyrene are present) which also gives the required levels of trap density. Mobile trapped charges do cause a type of hysteresis in the *C-V* curve, yet it is still possible to rule these out as being the source of the hysteresis for two reasons. Firstly, mobile charges take many minutes to move through the polymer layer under constant voltage stress, rather than the immediate effect that can be seen in the flatband voltage shifts here. Secondly, due to the slower movement of mobile charge through the insulator, the whole curve including positive and negative voltage sweeps moves, as distinct from the hysteresis shown here between the positive and negative sweeps.

To ascertain if gold nanoparticles can give the required levels of trap density the Langmuir-Blodgett gold nanoparticle films were investigated via atomic force microscopy. Figure 5.35 shows the topography image of a single monolayer of gold nanoparticles deposited on silanised silicon dioxide substrate.

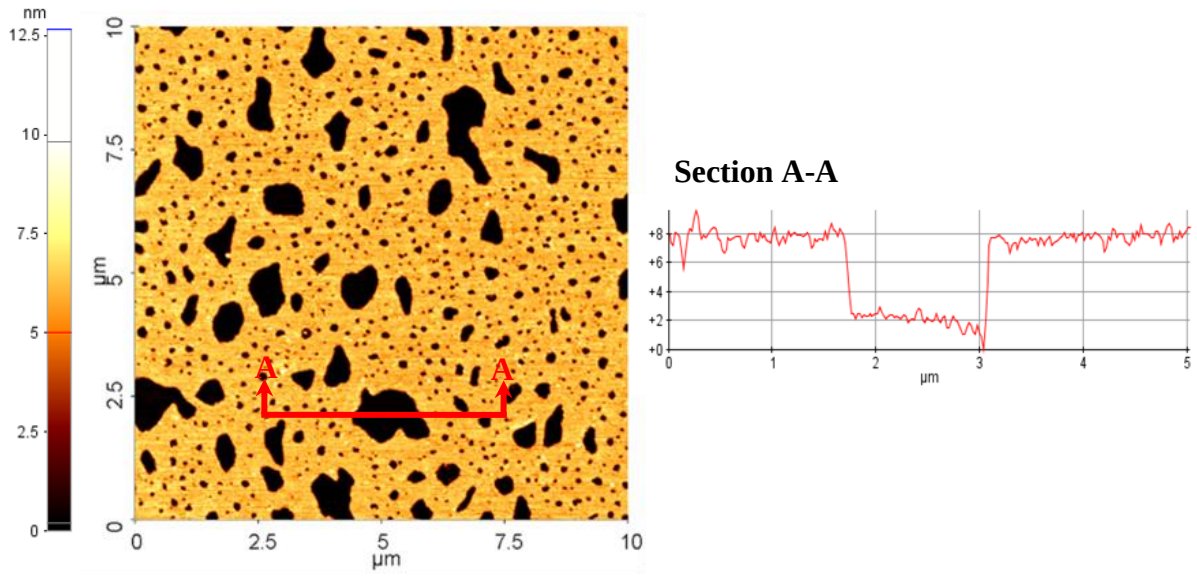


Figure 5.35 Topography AFM image of a gold nanoparticle monolayer deposited on silanised silicon dioxide.

It is clear from the figure that gold nanoparticles have deposited on the substrate material, with light areas of the image corresponding to the nanoparticles and the darker areas being the SiO_2 substrate. From analysis of this image and other images taken across the substrate the surface coverage is approximately 85%. From the Type-II nanoparticle certificate of analysis the diameter is ~4 nm [155], giving to a reasonable approximation $7.2x10^{12}$ nanoparticles·cm^{-2}. If it is assumed that one nanoparticle can contribute one trapped charge then the levels of trapped charge necessary for the hysteresis can easily be contributed by the nanoparticles.

Further proof that the gold nanoparticles are responsible for the hysteresis comes from comparing MIS capacitors including nanoparticles, to the hysteresis response from a capacitor on the same substrate, but without the gold nanoparticle layer (Figure 5.36). As these capacitors were fabricated on the same substrate as those shown in Figure 5.34 they underwent exactly the same processing stages and were fabricated to exactly the same specifications. This rules out the possibility that the hysteresis could be due to different processing conditions, or slightly different device geometries.

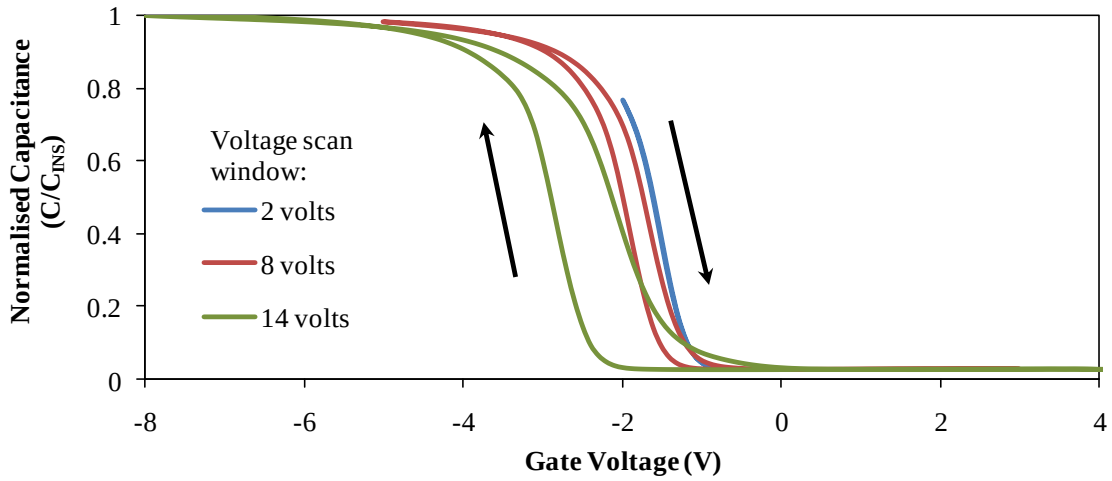


Figure 5.36 Hysteresis in an MIS capacitors without the nanoparticle layer. In all cases hysteresis was in the clockwise direction as indicated by the arrows. (Fabricated on the same substrate and with the same conditions as the device shown in Figure 5.34).

By comparing the hysteresis window (ΔV_{FB}) of the capacitors to the gate voltage scan window, as shown in Figure 5.37, the amount of hysteresis (and so the amount of trapped charge) increases as the gate voltage scan window is increased.

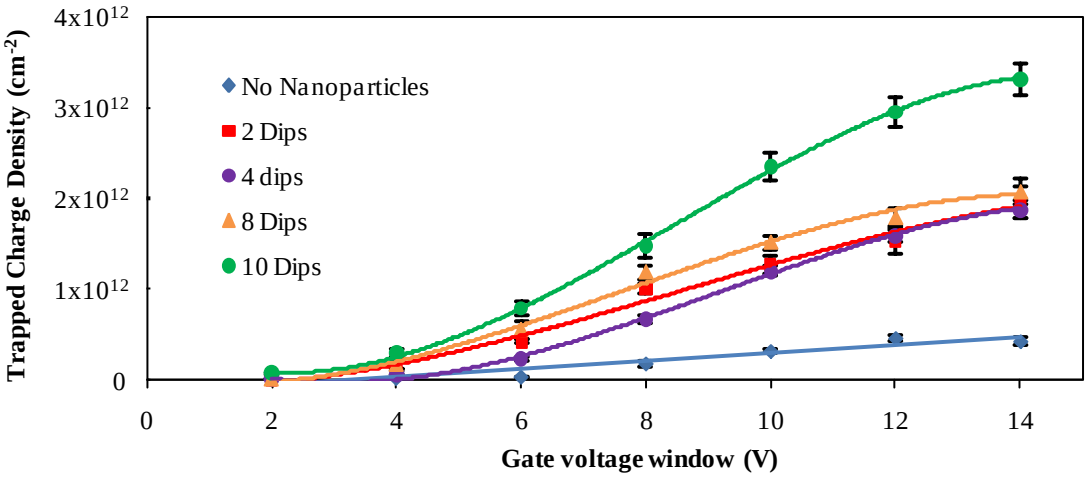


Figure 5.37 Hysteresis window and trapped charge density vs. gate voltage scanning window for different amounts of nanoparticle layers.

This also suggests that the charging of the nanoparticles is electric field induced, rather than due to an increase in leakage current passing through the capacitors. From Figure 5.33 the leakage current is largely independent of gate voltage until gate voltages >5 V are applied, while the electric field will increase linearly as the gate voltage is increased, giving a much better correlation with the observed increase in trapped charge density.

By comparing the hysteresis levels with the number of nanoparticle layers that each of the capacitors had during fabrication there is surprisingly little correlation between the higher number of nanoparticles present for the higher layer numbers and the magnitude of the hysteresis. The 2L, 4L and 8L devices all show similar levels of trapped charge considering the large increase in the amount of nanoparticles that are present, while the 10L device shows a disproportionately large increase in trapped charge over the other devices. It is possible to confirm that a greater number of dips does in fact correspond to a greater number of nanoparticles, by referring to the area versus time plots for the Langmuir-Blodgett depositions. Figure 5.38 shows the deposition characteristics for the 2L devices confirming that nanoparticles are being deposited on each dip, with deposition being X-type, i.e. nanoparticles are being deposited on the downward stroke only. Similar graphs for the 10L devices show that for higher numbers of dips the transfer ratio tends to decrease slightly and also some of the nanoparticles are removed on the upward stroke. This means for >8 dips further increases in the number of nanoparticles is actually minimal.

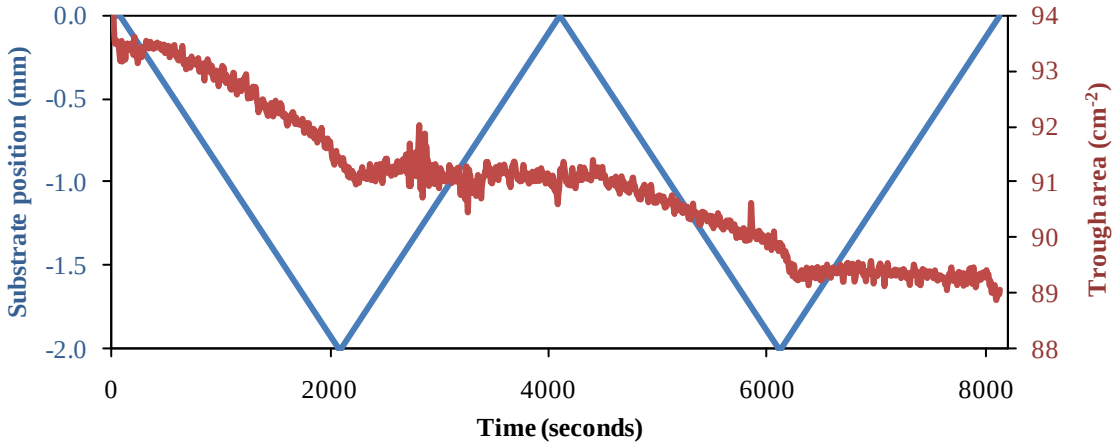


Figure 5.38 Area vs. time graph for a '2 dip' MIS capacitor, showing deposition occurred on each downward stroke of the substrate.

This makes the large increase in trapped charge between the 8L and 10L devices even more unexpected and suggests that there may be another mechanism responsible for the increase in trapped charge, rather than simply the physical number of nanoparticles present.

The reasons behind why the magnitude of hysteresis is not directly related to the amount of nanoparticles can be explained by further investigation of the absolute levels of trapped charge density that is present. Consider the following two examples; first the 2L devices at the maximum gate voltage scanning window, corresponding to the minimum amount of nanoparticles present in any of the capacitors measured. Here the levels of trapped charge are

approximately $2.0x10^{12}$ cm^{-2}. With an average nanoparticle diameter of 4 nm, this gives an approximate density of ~$7.2x10^{12}$ nanoparticles cm^{-2} assuming that only the nanoparticles in close proximity to the semiconductor-insulator boundary affect the voltage shifts. This means that only a fraction of the nanoparticles are contributing to the levels of trapped charge (~27% of the nanoparticles if each one is capable of storing a single electron). The second example is the 10L devices, where the maximum levels of trapped charge are present at $3.3x10^{12}$ cm^{-2}. For this density of trapped charge this is still only equivalent to ~47% of the nanoparticles being charged. If the majority of the nanoparticles are not being charged in the capacitors then the amount of hysteresis is not limited by the amount of nanoparticles, hence introducing more would not be expected to increase the levels of trapped charge significantly. Exactly why only a minority of the nanoparticles appear to be charging remains unclear. It is possible that it could be related to imperfections in the capacitor structure such as non-uniformities in the insulator thickness or pinholes and other defects in the insulator layer. Any areas of the capacitor where the insulating layer is thinner, or has defects will result in a localised increase in electric field. This is especially the case for any pinholes, which can result in significant field enhancement effects, leading to nanoparticles in these areas of the capacitor being charged at an earlier stage than the bulk of the capacitor.

This would also offer a further explanation for why there is a strong correlation between the amount of trapped charge and the strength of the electric field across the capacitor, as only certain areas of the capacitor would be experiencing field strengths high enough to induce charging of the nanoparticles. As the electric field is increased more areas would experience higher fields, hence more nanoparticles would become charged. In order to confirm this hypothesis an investigation was conducted into the quality of the evaporated PVP insulating layer from both 10L and 2L devices, i.e. a device that exhibited a large trapped charge density (10L) and one that had moderate trapped charge density (2L). The AFM topography images of the PVP layer of the 10L and 2L devices are shown in Figure 5.39(a) and (b) respectively, with significant differences found in the morphology of the two films.

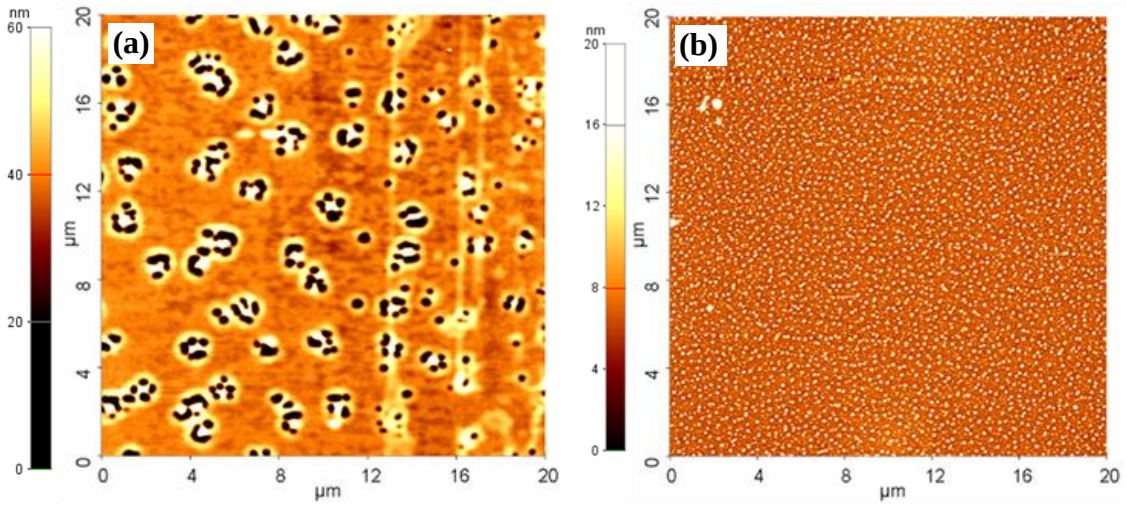


Figure 5.39 AFM topography image of the evaporated PVP insulator taken from (a) 10L devices and (b) 2L device.

It is immediately evident that the quality of the PVP layer in the 10L devices is significantly lower than that of the 2L device, with a large density of pinholes and defects. It is likely that the increased amount of trapped charge is as a result of higher electric fields in the defect areas resulting in greater numbers of nanoparticles being charged. These pinholes are not believed to penetrate the full depth of the PVP layer, with depths of approximately 30 nm measured from the AFM images (vs. 50 nm PVP film thicknesses). Provided the electric field strength doesn't exceed the dielectric strength of the PVP, these defects are not likely to prove detrimental to the devices, and in the devices tested there was no evidence of dielectric breakdown (no large increase in leakage current, drop in capacitance or damage to the top electrode).

One further piece of information that can be extracted from the *C-V* characteristics is the nature of the charges that are being trapped. In the majority of the work published on nanoparticle based PMDs it is claimed that electrons are being stored on the nanoparticles, with the electron being supplied from an electron donating species that is also present in the memory device, such as 8-Hydroxyquinoline [9-10], the nanoparticle capping ligands [16], or from the polymer chain of the insulator material [15, 94-95]. There are however a minority of papers where a storage of holes on the nanoparticles is proposed [88, 156]. By considering the position of the *C-V* curves in relation to the theoretical curve with no trapped charges present it can be deduced whether the trapped charge is positive or negative, as illustrated by Figure 5.40.

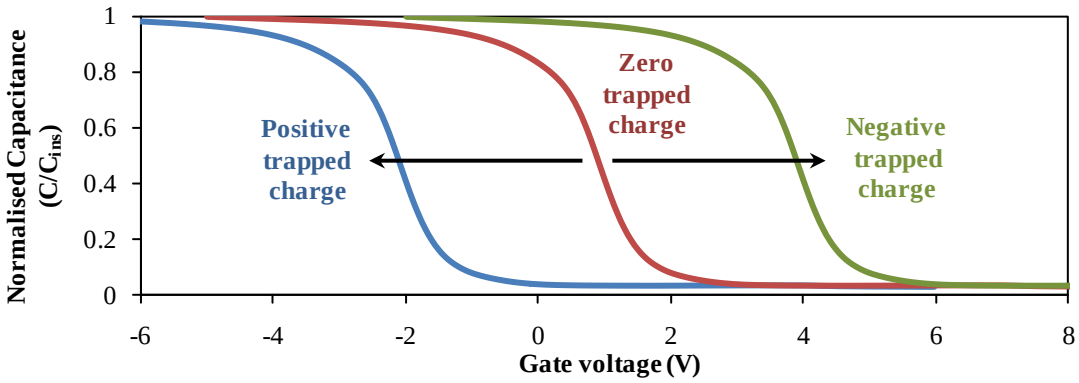


Figure 5.40 Effect on the *C-V* curve of positive and negative trapped charges.

Leong *et al*. [88, 156] used the argument that the clockwise hysteresis present in their devices was proof that holes were being trapped on the nanoparticles. This argument is however flawed. The hysteresis direction can give information regarding whether the charge is being injected through the SiO_2 insulator, or through the polymer insulator layer, but the type of charge is dictated by the position along the gate voltage axis of the *C-V* curve. This can be best demonstrated by considering the four examples shown in Figure 5.41.

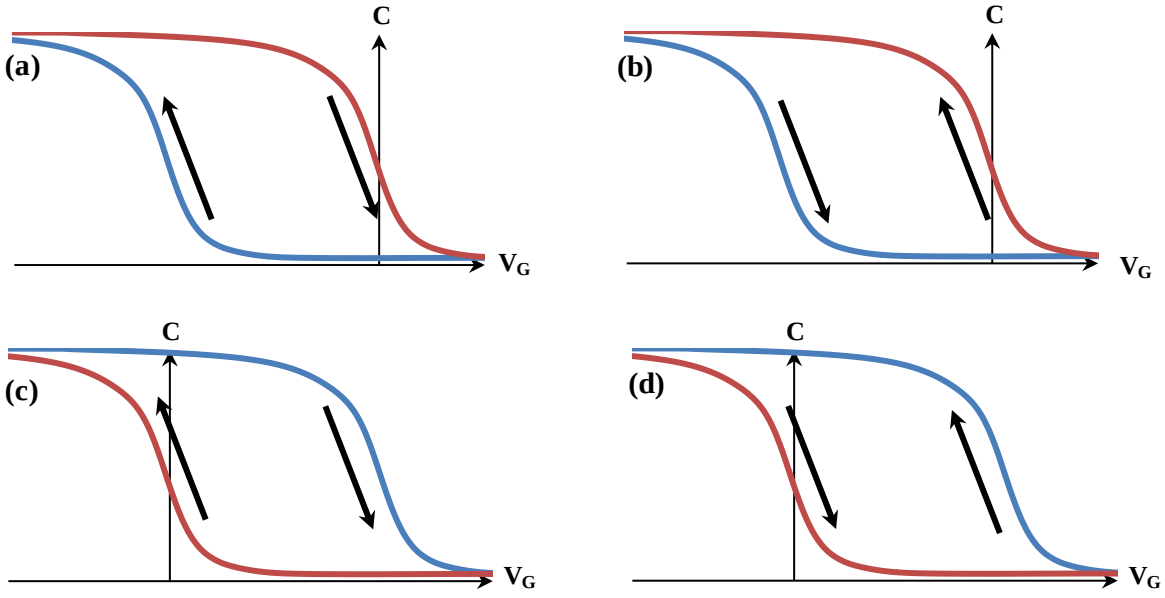


Figure 5.41(a) Holes trapped, injected through polymer insulator. (b) Holes trapped, injected through SiO_2. (c) Electrons trapped, injected through polymer insulator. (d) Electrons trapped, injected through SiO_2.

If holes were being trapped on the nanoparticles (resulting in a net positive trapped charge) Figure 5.41(a) or (b) would result. If clockwise hysteresis is present then the holes are being trapped under a positive gate voltage, which necessitates the holes being injected

through the polymer insulator. Conversely if the hysteresis is anticlockwise then the holes have to be injected under a negative gate bias so are being injected from the silicon through the SiO_2. Figure 5.41(c) and (d) show the consequence of electrons being trapped resulting in a negative trapped charge. Clockwise hysteresis means electrons are being trapped under negative gate biases, so injection is through the polymer insulator.

By considering data presented in Figure 5.34, the curve for a 2 volt gate window scan is approximately in the expected position for an ideal capacitor. For larger gate voltage windows, when hysteresis is present, while there is a small shift towards more negative gate voltages in the *C-V* characteristics, the majority of the hysteresis extends into the positive gate voltage regions. This matches closely with the situation in Figure 5.41(c) indicating that in these devices the gold nanoparticles are trapping electrons, and that they are being injected through the polymer layer from the gate electrode. This is also consistent with the data collected in §5.2.4.3 where it was found that the nanoparticles were able to store a greater amount of negative charge than positive charge.

5.3. Filamentary Formation

Some research groups theorise that the high *on* state currents are due to filamentary formation, which if some simple calculations are performed can be shown to be capable of supporting these levels of current. For instance, if the filaments are metallic in nature and are assumed to originate from the aluminium electrodes, then a simplistic model for the size of conducting area can be obtained from the Preece equation [157] which states that:

$$I = K \times d^{1.5} \qquad \textbf{Equation 5.10}$$

Where I is the melting current of the filaments, K is a materials based constant (59.3 for aluminium [158]) and d is the total conductor diameter in mm. For a current of 1 mA this would require a total conduction diameter of 0.66 μm. If each filament is assumed to be of nanometre dimensions (1 nm diameter) and the total device area is 1 mm^2 [7], then to support this level of current only one, 1 nm diameter filament would be required per 9.25 μm^2 of device area, which is a relatively low filament density, and easily conceivable. If gold is assumed to be the conductive material (originating from the gold nanoparticles), then as the melting temperature and conductivity is higher, for the same current of 1 mA less material would be expected to be necessary, hence the filament density would be less than for aluminium.

Attempts have been made by researchers to find and image these conductive filaments, as discussed in §2.3.2 in relation to resistive switch devices, but there is still only circumstantial evidence existing for the presence of filaments in PMDs. Possible sources for the filamentary material have been identified as either from the electrodes, metal nanoparticles, or decomposition of the polymer layer into carbon. As switching is not limited to carbon based polymer insulators, and also not limited to the inclusion of nanoparticles, it will initially be assumed that if filaments exist, then the electrodes are the most likely source of the conductive material. Considering that this may be the case, there has been relatively little research conducted into the evaporation process and metal used for the fabrication of the electrodes. Bozano *et al*. did conducted a large study into the type of metal nanoparticle used and the metal used in the bottom contact, with materials including magnesium, silver, aluminium, gold, chromium and copper investigated. They found that bistability was common among all the materials with the exception of gold, which resulted in shorted devices. Only evaporated aluminium top contacts were investigated though, so it was not possible to draw conclusions about the role of the top contact metal. Similar results for gold and chromium top contacts have also been found in the experiments conducted in §4.3.2, where all the devices fabricated were shorted together and ohmic behaviour measured. This is in contrast with some of the earliest work on electroformed devices (§2.3.2) where gold electrodes were found to be critical to the forming process [57], however in these early devices inorganic insulators were used with film thicknesses considerably greater than those present in recent devices. Results here with gold or chromium electrodes and polymer insulators suggest that some metals can penetrate deep into the polymer layers, either during the evaporation process itself, or through migration under the application of an electric field. Experimental evidence suggests that the former of the two mechanisms is predominant, due to the electrodes being shorted at low voltages during the initial voltage sweep. Additional evidence comes from experimental results in §4.3.2 showing that the top contact material is the most important, with, for example, chromium as the bottom contact making viable devices, and chromium as the top contact resulting in shorted devices. This would suggest that these metals have already penetrated the full depth of the polymer before any application of an electric field. If migration were responsible then the devices would not be expected to be shorted during the initial voltage sweep, and then short at a given applied voltage. This implies that it is the evaporation process that is responsible for penetration, possibly with further migration occurring under higher voltage biases. From experimental data obtained for

this investigation it is possible to conclude that gold and chromium can readily penetrate polymer layers up to 50 nm thick (the maximum polymer thickness used in test devices).

Some work has been carried out to investigate the effects of different deposition techniques on the memory effect, with Kim *et al*. [159] investigating both thermally evaporated and electron beam deposited top aluminium electrodes. They concluded that evaporated contacts were necessary for high *on/off* ratios and reproducible characteristics, due to the formation of aluminium nanocrystals embedded in the polymer layer during the evaporation process, which they claim are essential for bistable characteristics. This leads to the possibility that in all reported memory devices there could be significant a amount of damage taking place between the polymer and the electrode material, which could be exacerbated by the choice of electrode material and the deposition process.

In many reports it is stated that slow evaporation rates are used, with typical rates of only a few angstroms per second [12, 86]. For electrode thicknesses of 100 nm this results in evaporation lengths in excess of 5 minutes. The implied assumption in many studies is that a slow evaporation rate results in top electrodes with a lower surface roughness and also a better quality interface with the polymer. However, for longer evaporations the temperature rise inside the evaporation chamber cannot be ignored. To ascertain whether this temperature rise could be significant an investigation was carried out to measure the maximum temperature experienced by the substrate material during the evaporation process. To accomplish this two analogue temperature sensors were placed inside the evaporation chamber via an electrical feed-through and connected to a data logging system, as shown in Figure 5.42.

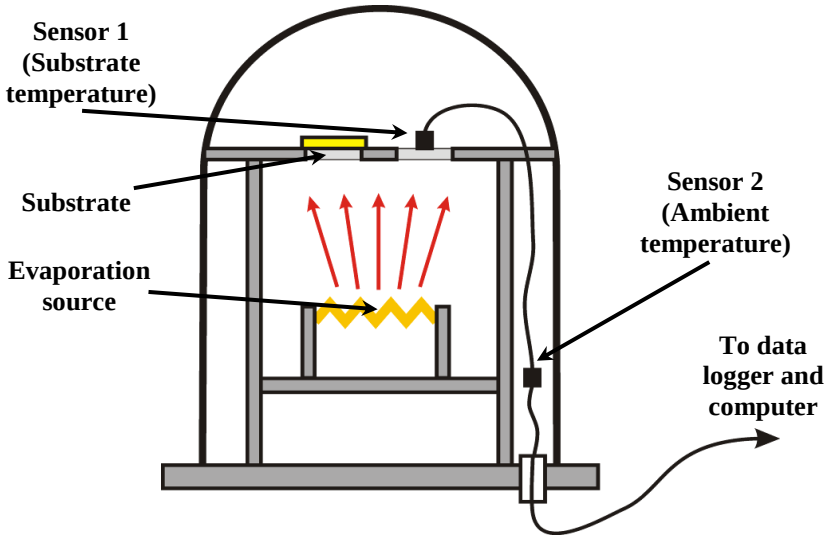


Figure 5.42 Measurement setup for evaporator temperature rise.

The two sensors were positioned so that one was shielded from the evaporation filament and measured the ambient chamber temperature, while the second was positioned as close as possible to the substrate material. This second sensor then also underwent the same metal deposition process as the substrate in order to estimate the substrate temperatures experienced during the evaporation. In all cases a 60 nm thick layer of aluminium was evaporated, the results of the substrate temperature rise experiments at evaporation rates of 1, 4 and 15 Å·s^{-1} are shown in Figure 5.43(a), while the ambient chamber temperature is shown in Figure 5.43(b). All the evaporations were conducted at pressures below 5x10^{-6} Torr, commenced at ~25 °C at zero minutes and had an approximate end time of the evaporation as indicated on the time axis.

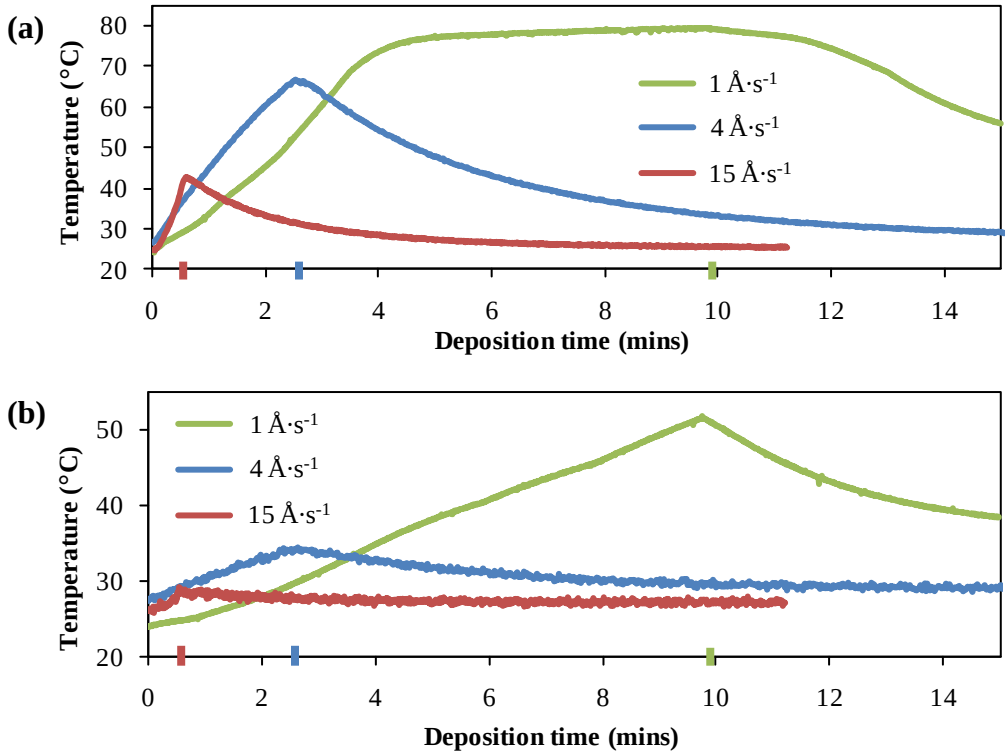


Figure 5.43(a) Temperature rise of substrate. (b) Ambient chamber temperature. Marks on the time axis indicate the times when the metal deposition was discontinued.

As would be expected, the slower the evaporation rate, the greater the temperature rise in the chamber. For the slowest evaporation rate of 1 Å·s^{-1}, which is common among reported devices, the temperature of the substrate (and hence the temperature the polymer material is likely to experience) reached ~80 °C. At these temperatures the possibility of annealing effects, metal penetration and reactions between the evaporated metal and the polymer cannot be ruled out. The temperature rise for this situation was also found to be non-linear, with the

temperature rapidly reaching 70 °C in under 4 minutes before plateauing. For this evaporation rate the ambient chamber temperature was also found to rise substantially, reaching ~50 °C by the end of the evaporation. These results show that to keep the temperature rise minimal the evaporation has to be completed within approximately 1 minute. To accomplish this a high evaporation rate of 15 $Å \cdot s^{-1}$ needs to be used, with the substrate temperatures in this case reaching 43 °C and ambient chamber temperatures rising to 29 °C. These are temperatures that are less likely to result in unwanted interactions between the metal and polymer. However, the effect of metal penetration at higher evaporation rates is unknown. The possibility of higher kinetic energies of the evaporated metals at higher evaporation rates could mean that metal penetration and nanoparticle or nanocrystal formation is still present and is an unavoidable side effect of the evaporation process. There is some evidence to support this with Dimitrakis *et al*. [160] reporting that higher evaporation rates of 25 $Å \cdot s^{-1}$ actually resulted in a more pronounced NDR region.

From both the experimental results discussed in this section, and the published data discussed here there is strong evidence that metal can penetrate deep into the polymer layer during the fabrication of the top electrode. Energy dispersive x-ray (EDX) analysis performed by Terai *et al*. [161] also confirms this for silver top electrodes, with silver being detected to depths of 75 nm into the polymer layer. What is unclear from these studies is whether this metal does form a continuous network, which would indicate a high likelihood of filament formation, or whether the metal is composed of discrete metal islands embedded in the polymer. The general consensus appears to be the latter, with the possibility of filaments forming under high electric fields. Despite this, there has been little success in imaging an individual filament with any of the scanning microscopy techniques (SPM, SEM or STM). Infrared spectroscopy has been used by Cölle *et al*. [17] to image the temperature rise at the points where current is flowing in the electrodes. They found that conduction only occurs in specific areas of the device and that switching occurs in the same location for subsequent memory cycles. It is presumed that, at these conduction 'hotspots', there are filament formations, but all that can be proved is that current is flowing in these areas. Similar methods have also been used by Jakobsson *et al*. in relation to the switching in molecular electronic devices based on Rose Bengal [81]. Promising experimental results for the imaging of filaments were reported by Baek *et al*. [162] by using the Current Sensing AFM (CS-AFM) technique. Here semiconducting polymer films of poly(o-anthranilic acid) (PARA) showed localised spikes in conduction when scanned over with the conducting AFM

tip. They attributed these spikes to areas where filaments had formed, but could not rule out the possibility that the high conductivity areas could be the result of morphological heterogeneities, or localised spots where the doping in the PARA could be higher.

In gold nanoparticle containing devices, it was regularly noticed that areas of physical damage became apparent on the top electrode at voltages much lower than would be expected for the dielectric breakdown of pure polystyrene films. In the majority of these cases there was actually no evidence in the *I-V* characteristics for a sudden switch to a higher conductivity state, however, in a small minority of devices single irreversible switching events did take place to higher conductivity states. Despite the switching not being reliable, or reversible, it was assumed that if filamentary formation was taking place, the most likely place would be at the points where damage was occurring. A study was undertaken to use AFM and EFM techniques around these areas of damage to better understand the topographical features of the damage and the physical composition of the damaged area. To be able to perform this analysis it was necessary to remove the top aluminium electrode material, so AFM and EFM images could be taken of the actual polymer layer, to ascertain whether conductive areas were present after the damage had taken place. Ordinarily removing the top electrode without damaging the polymer layer would not be possible, however, devices were fabricated with a second, thin polymer layer of PVP. This was spin-coated to be as thin as possible, in order to minimise the possible effects on the *I-V* characteristics, with ellipsometer measurements indicating a thickness of 20 nm. Top aluminium electrodes were then evaporated as normal. The full device structure was as follows: 50 nm aluminium bottom electrode, 50 nm PS+NP, 20 nm PVP and 120 nm aluminium top electrode. As PVP is soluble in methanol and polystyrene is not, it is possible to remove the PVP layer and top electrode after the electrode damage has occurred, while still leaving the polystyrene layer intact to be analysed. As expected, even with the PVP layer the damage to the top electrode still took place, with damage becoming apparent at voltages greater than approximately 6 – 7 V. An optical microscope image of the damage on the top electrode can be seen in Figure 5.44(a), with the visible damage after removal of the electrode shown in Figure 5.44(b). The damage clearly penetrates through to the polymer layer.

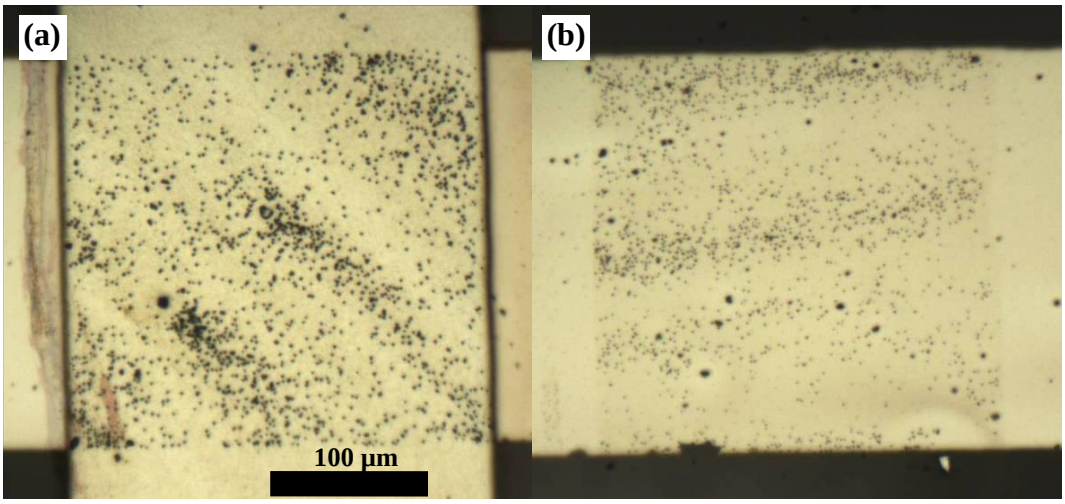


Figure 5.44 Optical image of damage to a stressed PMD: (a) Top electrode damage. (b) Middle polymer layer damage.

It is clear from the optical images that the damage is not just confined to the surface of the electrode, but the exact nature of the damage and the depth to which the damage penetrates cannot be determined from optical images. Upon studying the top electrodes with AFM it was discovered that not all the areas of damage were identical, with three distinct types of damage being distinguished. In order of severity, the first type of feature consisted of mounds on the surface of the top electrode, as shown in Figure 5.45.

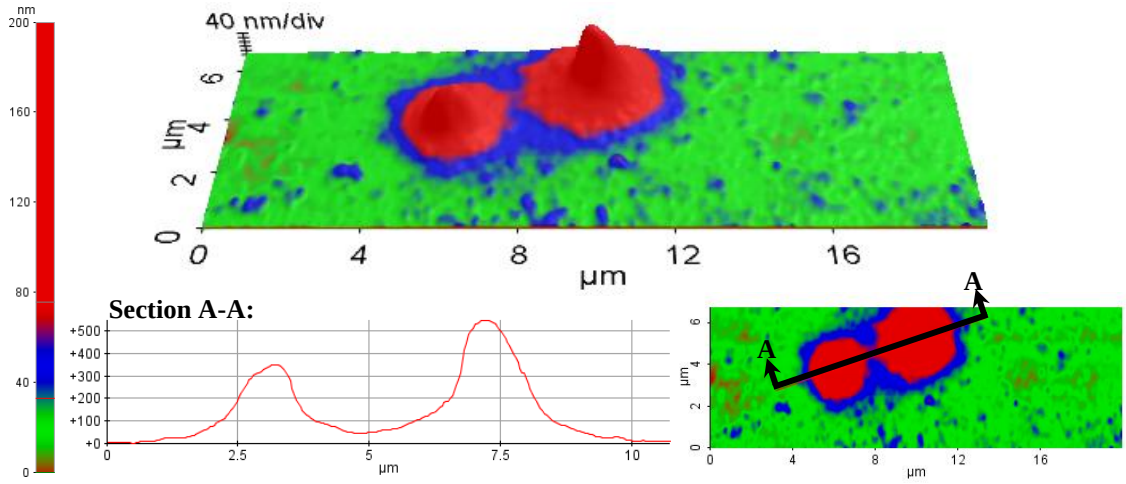


Figure 5.45 3D topography and line profile of the first damage type on a PMD's top electrode (Non-standard colours have been used to better highlight the features).

It is not clear with this first type of damage, whether it is indeed caused by applying a voltage across the device, or whether they are simply defects from the manufacture of the PMDs. It is quite possible that these features could be a result of unwanted particulates trapped under the top electrode. The second type of damage appears to be directly caused by

the voltage applied across the electrodes, with more pronounced mounds on the surface and evidence of rupturing on the top portion of the mounds, as shown in Figure 5.46(a).

From line profile measurements the depth of the rupture on the top surface of the mound measures approximately 150 nm, suggesting that the rupture extends down to the polymer layer underneath. However, the true depth could be greater than this, as for this image contact mode AFM was used and from the line profile the topographical features in the rupture appear to be limited by the shape of the AFM tip. An EFM image of the area also shows ambiguous results, as show in Figure 5.46(b), taken with the bottom electrode biased at 5 V. A strong EFM signal was obtained from the top electrode, which could indicate that the top electrode is shorted with the bottom electrode through the areas of damage. The actual mound itself did not show a high potential though, which could be an indication that the strong EFM signal is actually due to a material difference, and that the damaged area is no longer pure aluminium from the top electrode. This could be due to a mixing of aluminium and polymer material, or possibly the formation of aluminium oxide due to local heating caused by conduction through these areas.

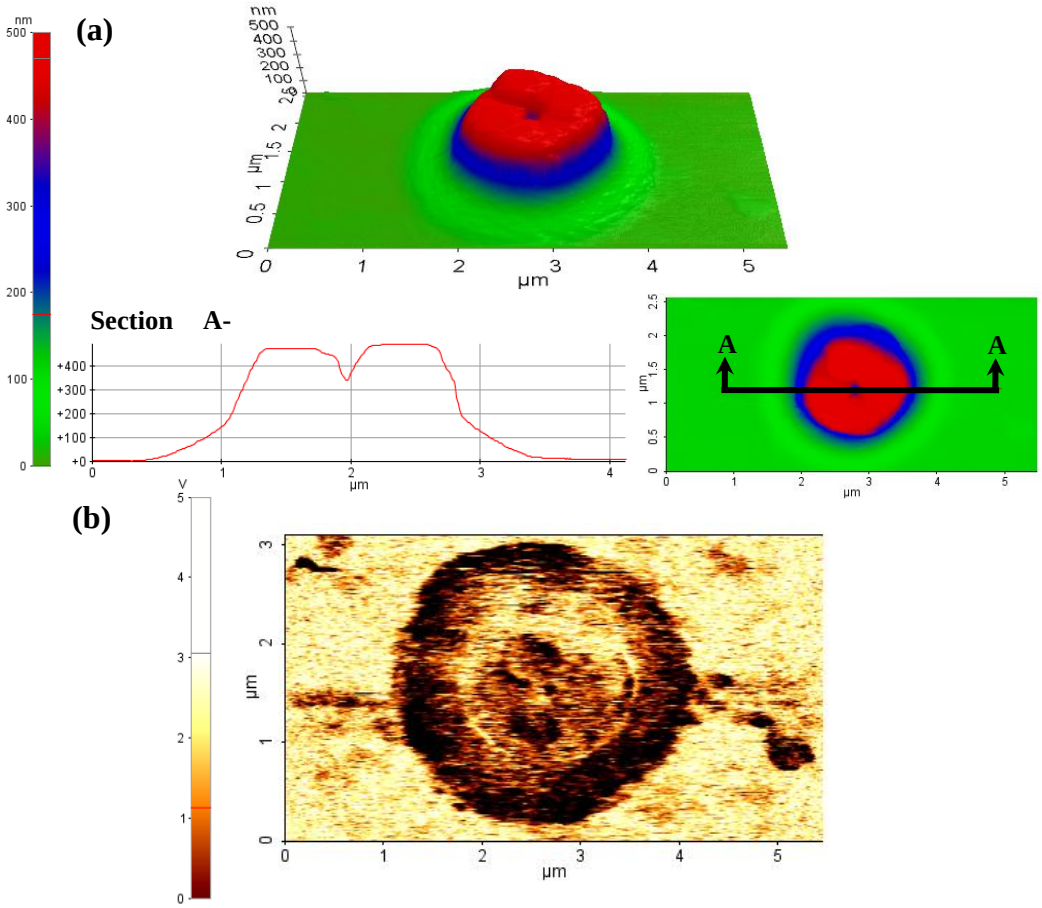


Figure 5.46(a) 3D topography and line profile of the second damage type on a PMD's top electrode (Non-standard colours have been used to better highlight the features). (b) EFM image of damaged area.

The third type of damage shows crater features (Figure 5.47), where material appears to have been ejected to form a ring structure around a central hole.

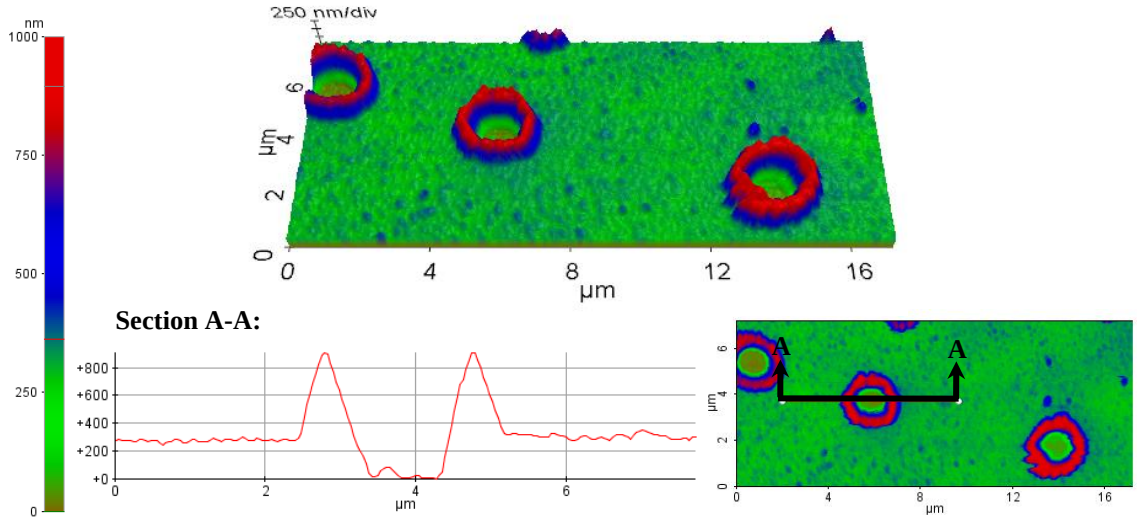


Figure 5.47 3D topography and line profile of the third damage type on a PMD's top electrode (Non-standard colours have been used to better highlight the features).

The line profile across one of these craters shows the middle area to be considerably lower than the surrounding electrode material, demonstrating that the damage extends into the polymer layer and also possibly through to the bottom electrode. In order to further investigate the depth and composition of these damage craters the top electrode and PVP layer were removed and further AFM and EFM images were taken of the polystyrene and gold nanoparticle layer (Figure 5.48(a) and (b) respectively).

From the line profile image the depth to the bottom of the crater is 100 nm, which as the polymer layer was only 50 nm thick, indicates that the damage also extends significantly into the bottom electrode. There is also a clear distinction in the AFM image between the polymer that was under the electrode, and the polymer that did not form part of the device (at a distance along the x-axis of approximately 6 µm). This damage could not have been caused by either the deposition of the PVP, or the subsequent removal of it and the top electrode, as both areas of polymer underwent these processing steps. The damage could either have resulted from the deposition of the top electrode, or from the voltages that were applied during the electrical stressing. In either case it shows that, not including the large crater features, significant damage is taking place in the polymer layer, with the route mean squared (rms) surface roughness increasing from 3.8 nm for the pristine polymer to 12.2 nm for the polymer in the device (once again not including the craters).

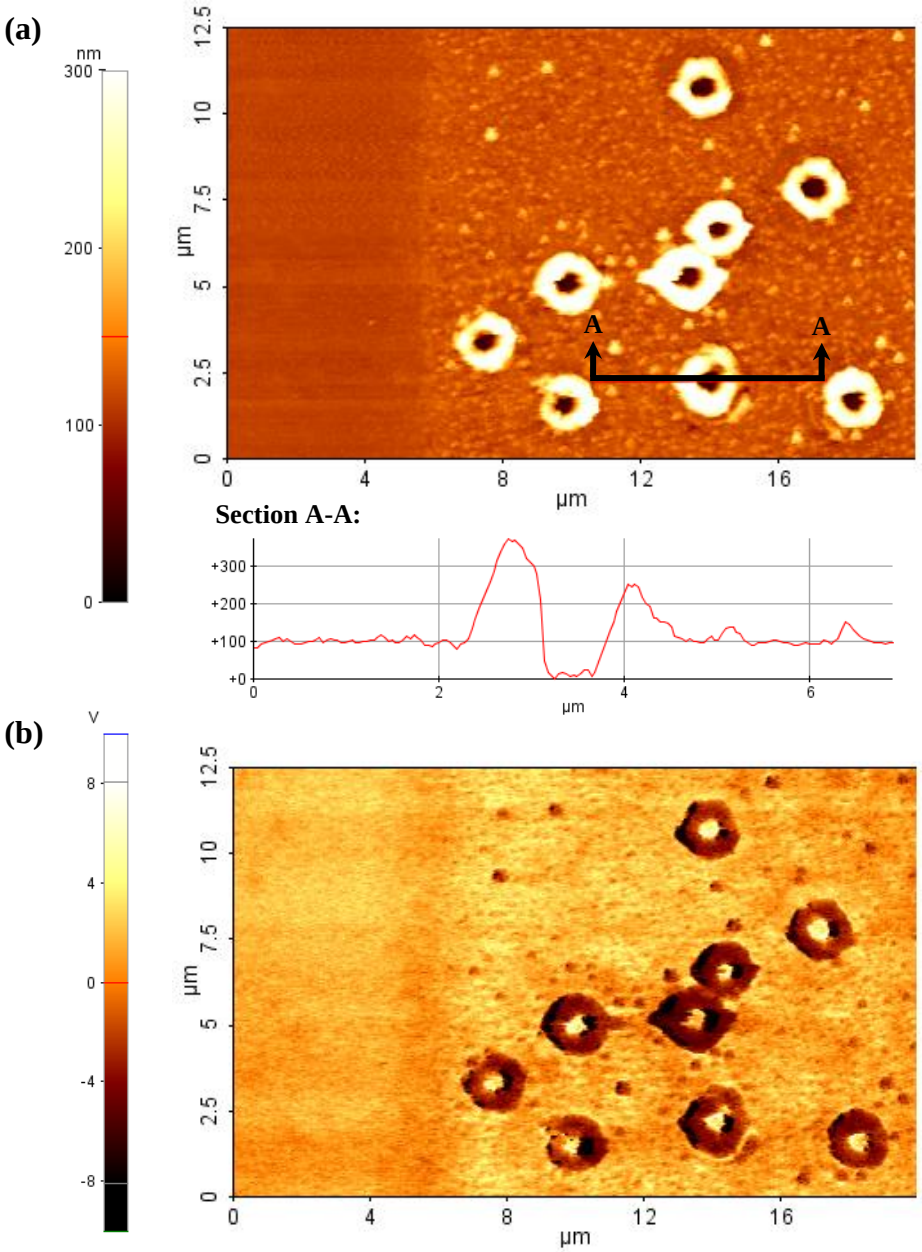


Figure 5.48(a) Non-contact AFM topography and line profile of PS+NP layer after removal of top electrode, and (b) EFM image of same area with bottom electrode biased at 10 V.

The EFM image of the damaged areas, taken with a bottom electrode bias of 10 V shows that the central areas of the crater are at a higher potential compared to the rest of the polymer layer, showing that the craters do penetrate through to the bottom electrode. There is also a good correlation between the topography image and the EFM image, with the higher features having a lower EFM signal, as would be expected for a thin insulator on a biased electrode. This also indicates that all the material present on the surface is insulating, hence there is no evidence in this image of any filamentary material. This is not necessarily surprising, as these

devices did not show any sudden switching phenomena, which could be indicative of filaments forming. Also if filaments are of nanometre dimensions then any response from them would be difficult to distinguish by the relatively low resolution of EFM images. At the maximum resolution of the EFM image (4096 pixels per scan line), to be confident of imaging nanometre sized filaments the maximum scan area would be ~800 nm^2. From the calculations at the beginning of this section concerning the possible density of filaments, statistically it would be unlikely to image a filament in this area. This also suggests a possible reason why other researchers have failed to image individual filaments.

Another aspect that is linked to filament formation, electrode penetration and nanoparticle inclusion in the polymer layer is the possibility of field enhancement effects occurring around any of these conductive materials in the polymer, whether introduced deliberately or by accident. A simple simulation showing the electric field enhancement between two metallic particles embedded in an insulator (i.e. gold nanoparticles in a polystyrene matrix) is shown in Figure 5.49, showing that the electric fields can be much greater than the average electric field strength would suggest. In this example two floating and uncharged 4 nm diameter metallic spheres are embedded in polystyrene, between electrodes 50 nm apart. The left electrode is biased at 10 V to give an average electric field of 2.0 $MV \cdot cm^{-1}$, however it was found in the simulation that the maximum electric field was actually 4.25 $MV \cdot cm^{-1}$. At these fields dielectric breakdown of the polystyrene is a strong possibility.

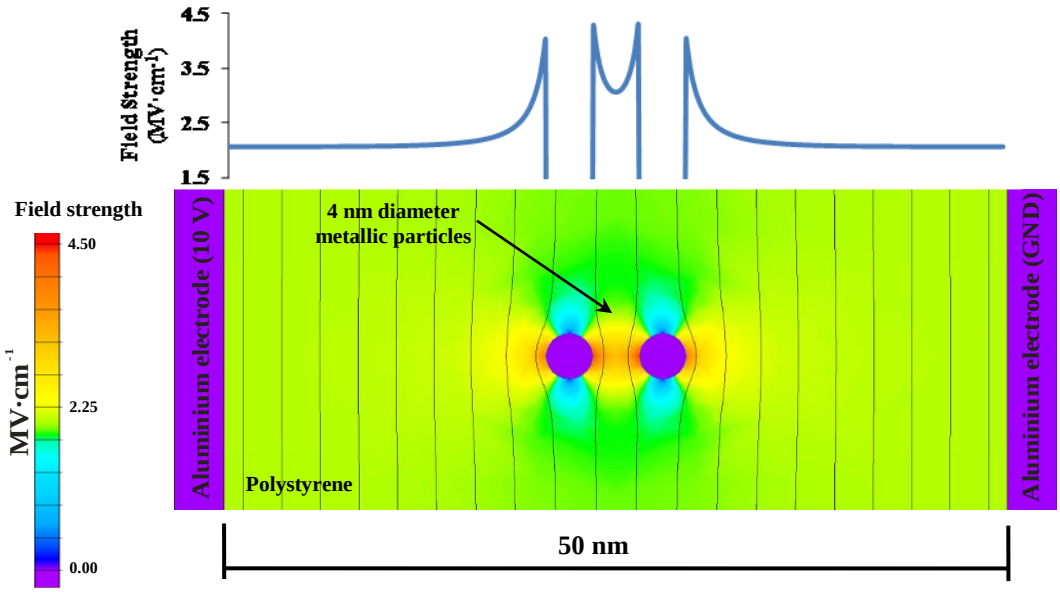


Figure 5.49 Electric field enhancement between two metallic particles in a polystyrene matrix.

In all the research referenced thus far it is assumed that the electric field across the PMD is uniform, however, this assumption is unlikely to be correct. Field enhancement is likely to have played a significant role in the damage that occurred to the devices studied earlier in this section, where the devices with nanoparticles included, showed damage at significantly lower voltages than would be expected for dielectric breakdown. In all PMDs including nanoparticles (and also any where metallic material has been introduced through top contact evaporation) there are likely to be significant field enhancement effects, which even at low voltages could result in electric fields greater than the breakdown fields for the polymer insulators. In a real device, field enhancement would be present between all nanoparticles, as well as any areas in the device where features are not homogenous, such as pin hole defects, dust particles and non-perfect interfaces between the contacts and polymer. This could readily lead to many networks of areas of field enhancement and areas where metal diffusion, filament formation, or dielectric breakdown can occur.

Further evidence for filamentary switching comes from the gold break junctions that are fabricated in §5.4. While the break junctions that had test materials and the junctions fabricated to be lateral PMDs, didn't show any evidence of switching, there were switching effects observed in an 'as fabricated' break junction before the deposition of any test materials. The *I-V* characteristics for this junction over the first three switching cycles can be seen in Figure 5.50, with the curves showing clear S-shaped characteristics. Specifically, they show an initial low conductivity state, with a sudden switch of many orders of magnitude (six orders in this case) to a current in the microampere range. There is no evidence of NDR and the low conductivity state can then be returned by applying a voltage of the opposite polarity.

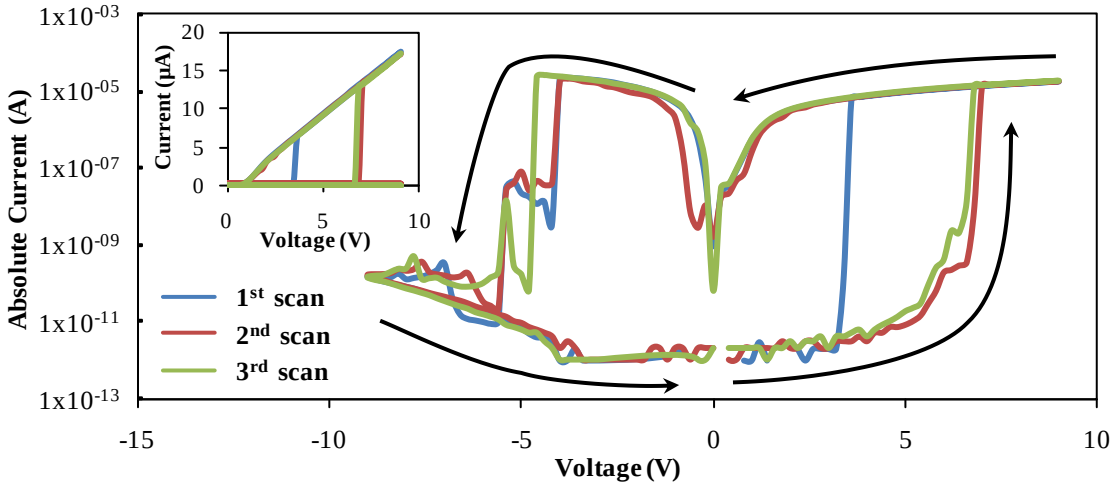


Figure 5.50 Switching characteristics in the *I-V* curve of an empty gold break junction. Arrows indicate the voltage sweep directions. Inset show the switching and current in the on state.

As the electrodes did not have any material deposited between them the only possible source of conductive material is from the electrodes themselves. This is also confirmed by the ohmic characteristics of the *I-V* curves in the *on* state, as shown in the inset of Figure 5.50. The break junction was also subjected to a series of *read*, *write* and *erase* (RWE) cycles to further assess the performance with the results of five of these cycles shown in Figure 5.51. Out of a total of 30 cycles that were applied to the junction switching occurred in 23, showing that reproducible switching is possible from a filament bridge.

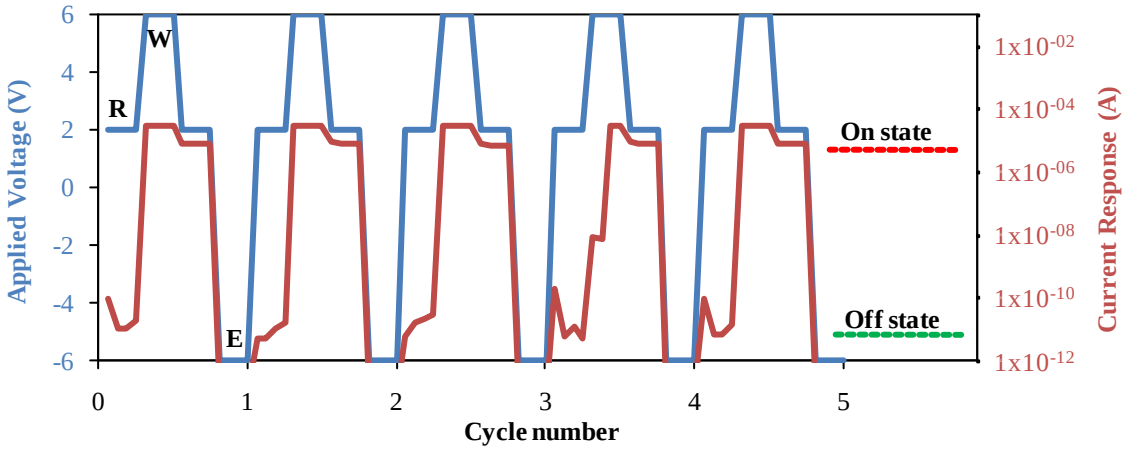


Figure 5.51 *Read*, *write* and *erase* cycles for switching in the break junction.

5.4. Conduction Characteristics of Constituent PMD Materials and relation to PMD *On/Off* Ratios and Current Density

One of the most prominent features of many of the PMDs that have been reported are large *on/off* ratios, which usually correspond to large currents passing through the devices in the *on* state. Indeed there are several reports of currents in the microamp range [8-10, 15], and even into the milliamp range [7, 12, 16-17].

The two most prevalent theories for the origin of these high current levels are; the formation of conducting filaments, as discussed in §5.3, or alternatively, quantum tunneling of electrons between either the nanoparticles in the device or the electron donating species. The first step in determining whether tunneling is a likely mechanism is to estimate the distance between the tunneling sites. By using the nanoparticle and polymer quantities from the paper by Ouyang *et al*. [9], with the estimation based on 4.08 nm diameter nanoparticles, and also assuming a uniform distribution throughout the memory device, then a spacing between nanoparticles on the order of ~1.5 nm could be expected (See Appendix F4 for

calculation). At these distances it is possible that tunneling could occur between the nanoparticles.

To experimentally determine whether these levels of current could be provided by a tunneling mechanism, structures based on metal break junctions were fabricated to investigate the *I-V* characteristics of gold nanoparticles. These test structures had densely packed nanoparticles deposited between the electrodes to give the maximum possible current that can be transported by the gold nanoparticles. In a PMD the nanoparticle density will always be lower than in these test structures, so by comparing the experimental levels of current to those reported in literature it is possible to draw conclusions about the likely levels of current from nanoparticle PMDs. Break junctions with 8HQ, polystyrene and nanoparticle admixtures were also investigated to closer simulate PMD structures and investigate the role that the constituent materials play in the current transport.

For these devices it is imperative that only the characteristics of the nanoparticles are measured, with no possible influences from the metal contacts to the nanoparticles. This immediately precludes the use of conventional vertical structures where nanoparticles are deposited on a bottom electrode, followed by thermal evaporation of a top electrode for two reasons. Firstly evaporated metal contacts are likely to penetrate the nanoparticle layer to some extent, and if any areas do not have complete nanoparticle coverage the electrodes will simply be short circuited together. At best, this produces results that are tainted by the influence of the metal electrodes penetrating into the nanoparticle layer, and at worst will simply measure the current passing through shorted electrodes. Secondly, in any thermal evaporation there will be some temperature rise of the substrate material (see §5.3) which may result in degradation of the nanoparticles. The solution to this is to use a lateral structure, while still maintaining approximately the same dimensions between electrodes (i.e. ~50 nm). Without using lithography techniques the simplest way to achieve these dimensions is with a metal break junction, where an electrical pulse is repeatedly passed through a thin conductor until failure and rupturing of the wire. At the failure point the resulting gap has dimensions of a few tens of nanometres, with an optical image of a completed junction shown in Figure 5.52(a).

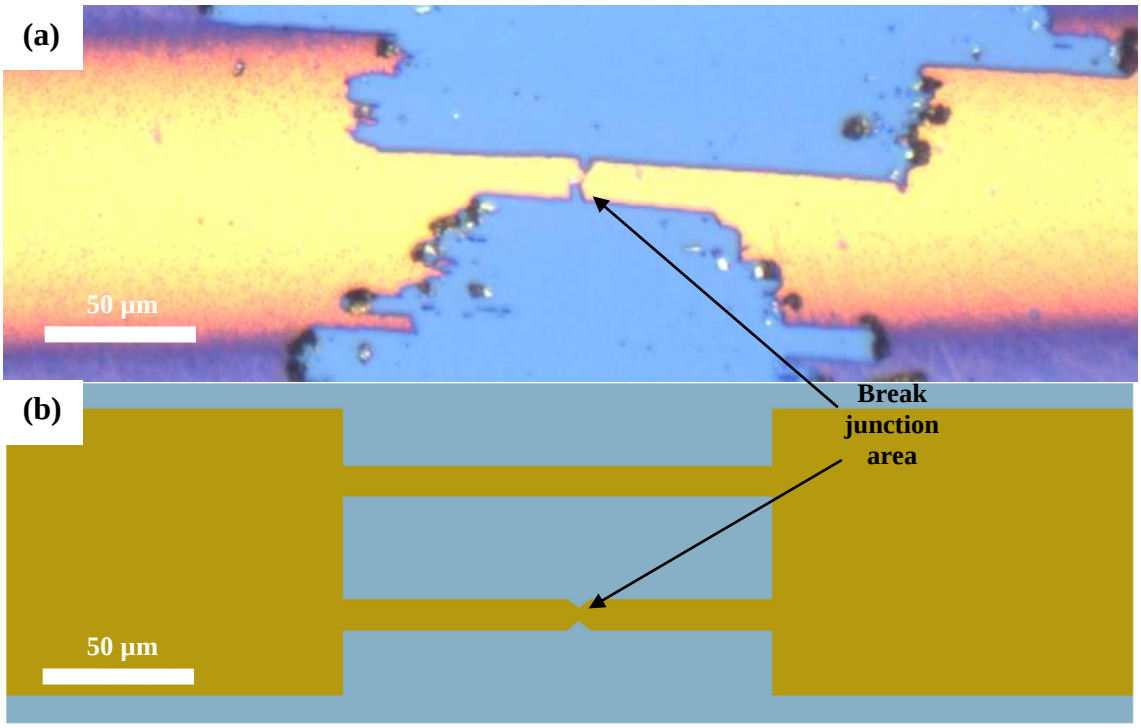


Figure 5.52(a) Optical image of a completed gold break junction. (b) Modified geometry allowing second current pathway.

Initial attempts at fabricating break junctions were made by evaporating 30 nm thick, 100 µm wide gold lines onto 100 nm thermally grown SiO_2. The line widths were then further reduced by mechanically removing the gold with a metal probe and manipulation equipment, leaving a neck in the line approximately 5 µm wide. Repeated pulses in the range of 25 – 35 V were then applied to the line. A physical break could be observed spreading across the junction under optical magnification, at which point the magnitude of the voltage pulses was reduced to complete the junction at a slower rate. However, it was found that in the majority of cases, at the point of failure the current density passing through the line was sufficiently high to vaporise the line, thus in effect acting like a fuse and destroying the break junction. To remedy this problem a novel geometry was designed to include two conduction paths on each line, as illustrated in Figure 5.52(b). With this geometry, at the point of failure of one line (where the break junction is formed) there is still sufficient metal remaining in the second line to support the current and so minimise the 'fuse' effect. The unwanted gold line was then removed leaving only the break junction behind.

AFM images of the break junction confirmed the dimensions of the gap to be approximately 20 – 40 nm. The EFM image confirms that there is no contact between electrodes, with the bottom electrode showing a different potential when a bias was applied

to the top electrode (Figure 5.53(a) and (b) respectively). Current-voltage characteristics were also measured for the break junctions, with any junctions having leakage currents in excess of $5x10^{-11}$ A being rejected. In the majority of cases however the leakage current measured was under $5x10^{-12}$ A.

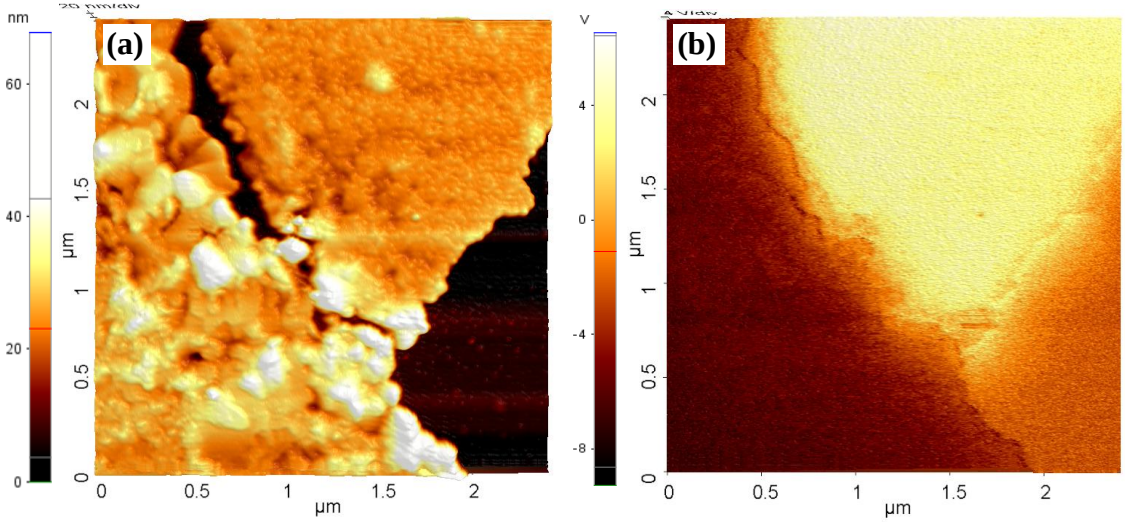


Figure 5.53(a) Topography image of break junction. (b) EFM image confirming the gap between electrodes.

Systematic investigations were carried out into the conduction of all the constituent materials that are found in gold nanoparticle PMDs by depositing the admixtures via drop casting between the electrodes and measuring *I-V* characteristics. In all cases Type-II gold nanoparticles and toluene solvent were used, with the materials/combinations of materials chosen for analysis shown in Table 5.2.

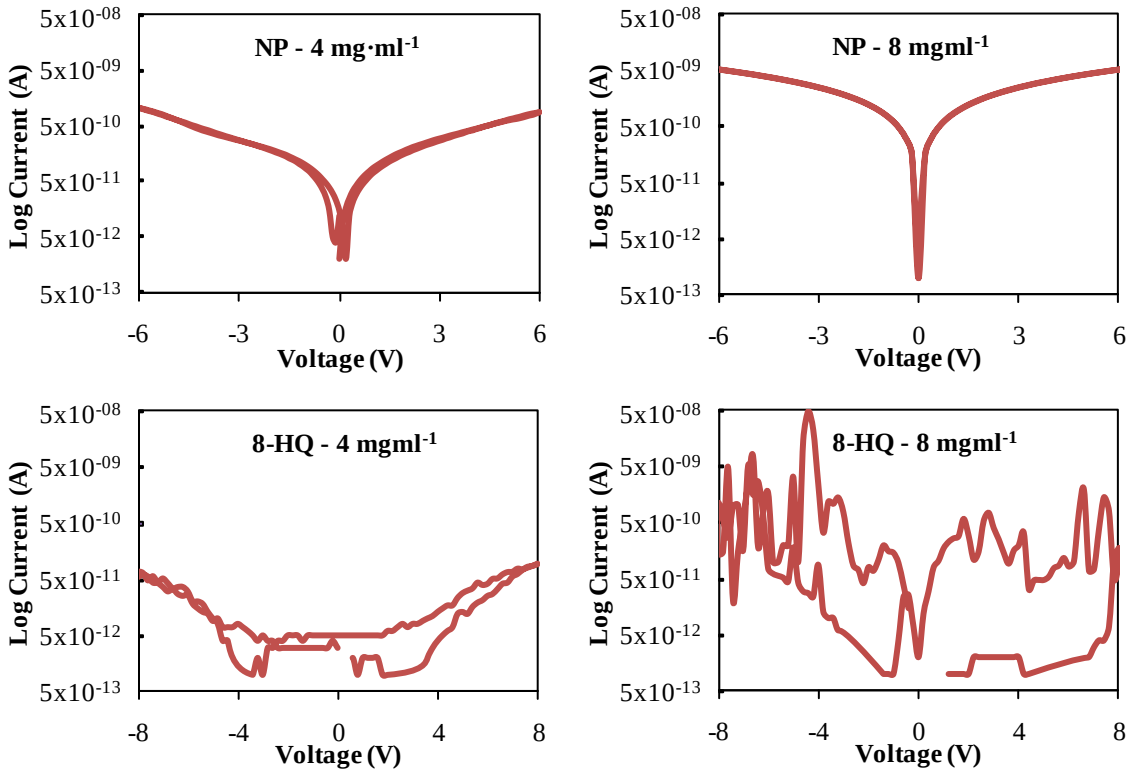
Table 5.2. Materials deposited for analysis in break junctions.

Material	**Material concentration (mg·ml^{-1} of solvent)**
Gold nanoparticles	4 & 8
8-Hydroxyquinoline	4 & 8
Gold nanoparticles + 8-Hydroxyquinoline	4 & 8
Gold nanoparticles + 8-Hydroxyquinoline + Polystyrene	4 & 8 NP & 8HQ, 12 PS

Typical *I-V* characteristics for all the material combinations are shown in Figure 5.54.This data does present the actual levels of current passing through the devices, rather than current density which is sometimes presented in published work. By considering the area of conduction in the break junctions, which is likely to be dominated by the area where

the electrodes are closest, this could lead to very high current densities, possibly of the order of several amperes per centimetre square. However, if tunneling is the main conduction mechanism in the *on* state of PMDs, then conduction would take place where the tunneling distance between nanoparticles is the least. This would be expected to result in the current being confined to small areas of the memory, making the current reasonably independent of device area. In this case it is possible to make a direct comparison between the magnitudes of current from the break junctions and the magnitudes of current reported in literature.

If devices containing only gold nanoparticles are considered first, it was found that by increasing the concentration of the solution the measured current also increased. Despite the devices only consisting of nanoparticles, by increasing the concentration of the solution it is likely that the nanoparticles will become more densely packed, leading to an increase in current. This device configuration is such that it is expected to result in the maximum amount of current possible for the nanoparticles to conduct. Despite this the levels of current measured are still many orders of magnitude smaller than the levels of current reported for the *on* state currents in many PMDs.



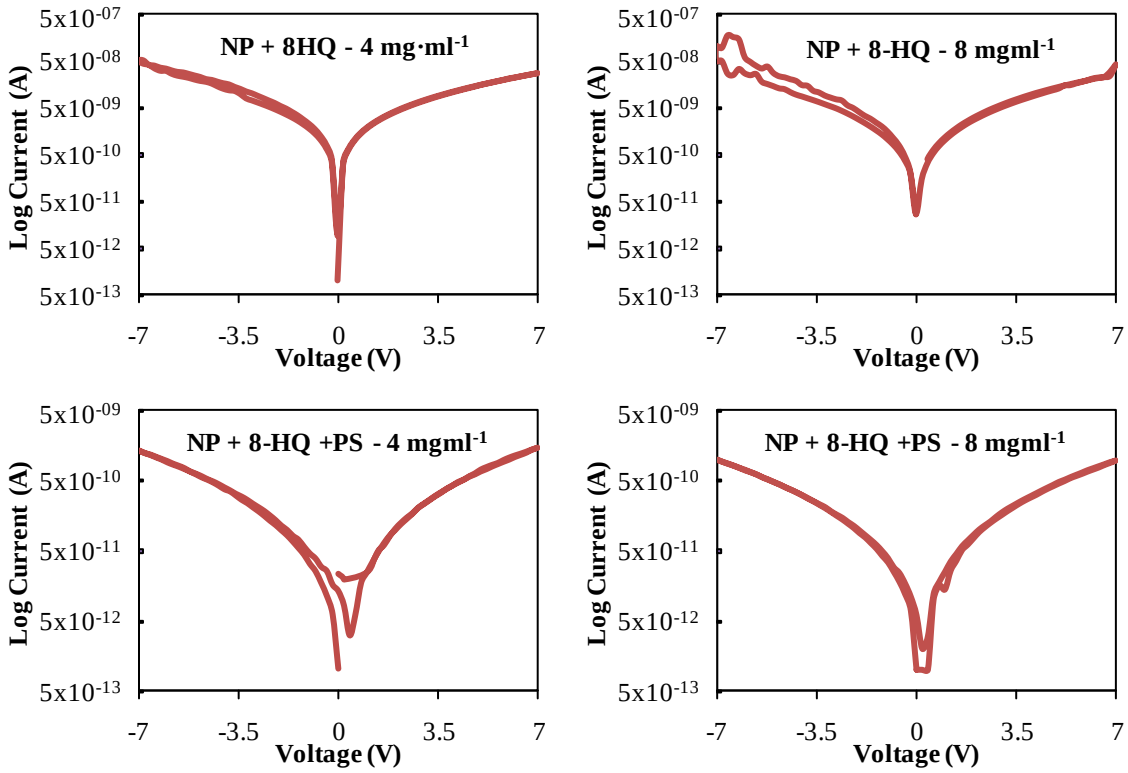


Figure 5.54 *I-V* characteristics of PMD constituents deposited between gold break junctions.

To confirm these levels of current, gold nanoparticles devices were also fabricated with a concentration of 20 mg·ml^{-1} of nanoparticles to solvent, resulting in a nanoparticle concentration significantly higher than any published PMD. It was found that even at these concentrations the current levels only increased by approximately an order of magnitude compared to a concentration of 8 mg·ml^{-1}, resulting in a maximum current of ~4x10^{-8} A at 6 V bias, still approximately two to four order of magnitude lower than the currents reported by Ouyang *et al*. [9, 16] and Lin *et al*. [15, 163]. The measurements taken from break junction *I-V* characteristics cast doubts over the nanoparticles, or any other constituent part of the devices being able to support these large current magnitudes, and indicates that some other phenomena is responsible when currents in excess of ~10^{-8} A are reported. It is possible that for these large currents there is some form of reversible breakdown in the polymer film and filamentary conduction, as discussed in §5.3. In this case these memories would then fall into the category of Resistive Random Access Memories.

Some published work, most notably that by Ouyang *et al*. [9] has theorised that in the high conductivity state tunneling between 8HQ molecules may be responsible for the high current. From the devices measured here when only 8HQ molecules were deposited between the electrodes it was found that current levels were the lowest of any configuration measured,

and also showed highly irreproducible characteristics. This suggests that any mechanism involving tunneling between 8HQ molecules in the *on* state is unlikely, especially considering the higher conductivity of the nanoparticles. The only justification for stating that tunneling between the 8HQ is the likely mechanism comes from the fact that if equal masses of 8HQ and gold nanoparticles are in a PMD, then due to the much lower mass of the 8HQ molecule compared to the nanoparticle, there would be a greater number of them, hence they would be closer together. For instance at a concentration of 4 $mg \cdot ml^{-1}$ of both 8HQ and 4.08 nm diameter nanoparticles, the estimated distance between 8HQ molecules would be ~0.2 nm (see Appendix F4 for associated calculations), while, as previously discussed, the nanoparticles would have a separation of ~1.5 nm, however, at these distances tunneling currents between nanoparticles could still be expected.

The break junction devices which model closest the configuration of PMDs are the devices with an admixture of nanoparticles, 8HQ and polystyrene (NP + 8HQ + PS devices) deposited between the break junction. These devices can in effect be considered to be lateral PMDs albeit one with a small cross-sectional area. With this in mind there is a great deal of information that can be extracted from the *I-V* characteristics in relation to the nature of the mechanisms that are responsible for the change in conductivity in conventional vertical PMDs.

In a lateral PMD switching and bistability would also be expected if nanoparticle charging is responsible for the large change in conductivity. All the constituent materials are present and the distance between electrodes is approximately the same as vertical PMDs, which should result in the charging of the gold nanoparticles and a change in conductivity upon the application of an electric field. However, in all the devices measured (eight devices in total between the two material concentrations used) no reliable switching took place between two different conductivity states. One device fabricated with a material concentration of 8 $mg \cdot ml^{-1}$ of 8HQ and gold nanoparticles did show one switch during an *I-V* sweep, as shown in Figure 5.55.

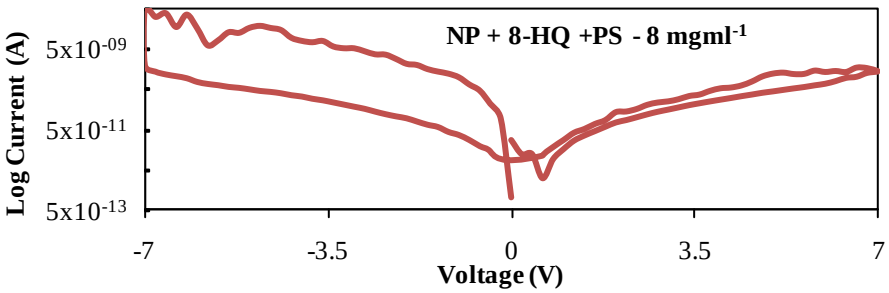


Figure 5.55 Single switch occurring in break junction lateral PMD.

This switch proved to be unreliable, with subsequent scans returning to the original characteristics, which indicates the switch was not due to a charging phenomena, as is the claimed mechanism in PMDs.

Another immediate feature is that the *I-V* characteristics for these lateral PMDs closely resemble the published results of vertical PMDs in the *on* state. (i.e. current is proportional to the applied voltage to a given power), which, if the nanoparticle charging theory is correct, would suggest that these lateral PMDs are already in their charged state in the as fabricated pristine condition. This is a feature that has never been reported in other PMDs, which are always in their *off* state when fabricated and there is no evidence to suggest that the nanoparticles here are charged prior to the application of an electric field. This would indicate that nanoparticle charging is not a prerequisite to the devices showing *on* state characteristics, and that actually this level of conductivity is the normal level for these admixture materials, with some other factor affecting the levels of current in the *off* state.

In some cases it is reported in the paper in question that the current increase is proportional to the voltage to a given power (i.e. $I \propto V^x$) [9-10, 14, 16, 98, 164]. However, in some cases only *I-V* curves are shown, and as these *I-V* curves usually show the log value of current it is generally difficult to ascertain whether the current follows a power law, or shows properties closer to ohmic conduction (i.e. linear increase in current with respect to voltage) [12-13, 95]. This is further complicated by the fact that some reported devices show NDR regions and N-Shaped *I-V* curves, while others show S-Shaped curves without NDR. As the lateral PMDs here showed no evidence of NDR regions, it is specifically S-Shaped PMDs that comparisons can be made with. For both concentrations of 4 and 8 mg·ml^{-1} of 8HQ and nanoparticles, the typical *I-V* characteristics show a very good fit with a relationship where current is proportional to the square of the voltage, as shown in Figure 5.56.

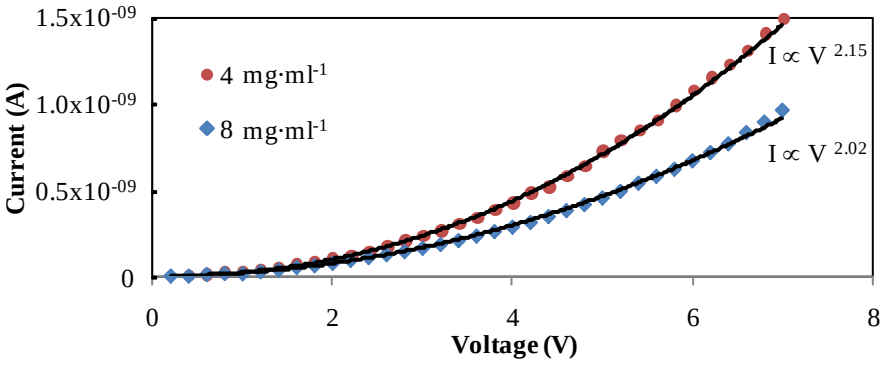


Figure 5.56 Data fitting for NP + 8HQ + PS typical device.

This suggests that the conduction through the device could either be Fowler-Nordheim tunneling or space charge limited conduction. Both of these conduction mechanisms have been proposed as the method of conduction in the *on* state of PMDs, and from a logical perspective both could be possible. In the case of Fowler-Nordheim tunneling, this is tunneling through a triangular barrier, which would be the expected situation at higher voltage biases, while for SCLC it has been theorised that if the nanoparticles are being charged this would set-up a space-charge field leading to SCLC [16, 164]. As there was no change in characteristics for the lateral PMDs, for the conduction mechanism here to be SCLC would require the nanoparticles to be charged in their as fabricated state before an electric field has been applied and, as previously mentioned, there is no evidence to suggest that this is the case. This would indicate that Fowler-Nordheim tunneling is the more likely conduction mechanism here, however it is difficult to differentiate between the two, as both mechanisms are also temperature independent.

There are also some reported S-Shaped characteristics which do not show a good fit to Fowler-Nordheim tunneling or SCLC. However, in papers by Ouyang *et al*. [9] and Yang *et al*. [14] they have fitted the characteristics to a combination of direct and Fowler-Nordheim tunneling and then also presented data showing the current was reasonably temperature independent as further evidence for a tunneling mechanism. The justification behind this combination is that in the low voltage region the tunneling is likely going to be through a square barrier, while at higher voltages tunneling through a triangular barrier will dominate. From the data presented in the paper it appears that a combination of the two tunneling mechanisms does result in a good fit to the data. Without completely reconstructing the data values from the graphs presented in the paper it is not possible to formulate the exact relationship that fits their data, however, the break junctions containing only gold nanoparticles appear to follow a very similar data trend and so will be used as an example of the problems with the data fitting attempted by Ouyang *et al*. The data presented in Figure 5.57(a) shows the experimental *I-V* curve for 4 $mg \cdot ml^{-1}$ gold nanoparticles deposited in a break junction, along with data fittings for an assumed tunneling mechanism of both direct and Fowler-Nordheim tunneling.

It is evident from the data that neither tunneling mechanism fits the data particularly well, and so Ouyang *et al*. attempted a simple addition of the tunneling currents. If the simplified expressions for tunneling currents (see §3.1) are taken then the combined current then takes the form:

$$I = C_1V + C_2V^2e^{-C_3/V} \qquad \textbf{Equation 5.11}$$

Using this combination it is possible to get a good data fit, as is shown in Figure 5.57(b), however, there are several reasons why this method cannot be used as proof of a particular conduction mechanism.

Firstly, a simple addition of the two different tunneling mechanisms would not be expected. A more likely combination would be a biased addition of the two, so at low voltages a greater proportion of the current would be from direct tunneling, while at higher voltages Fowler-Nordheim tunneling would contribute the majority of the current. Secondly, from a mathematical perspective, Equation 5.11 is simply fitting a polynomial equation to the data. As the data would be expected to be a second order polynomial, any equation that has a voltage term and a voltage squared term will provide a good fit to the data. This means that it would be equally possible to fit a combination of direct tunneling and SCLC to the data, which would also match with the temperature independence of the current that has been reported.

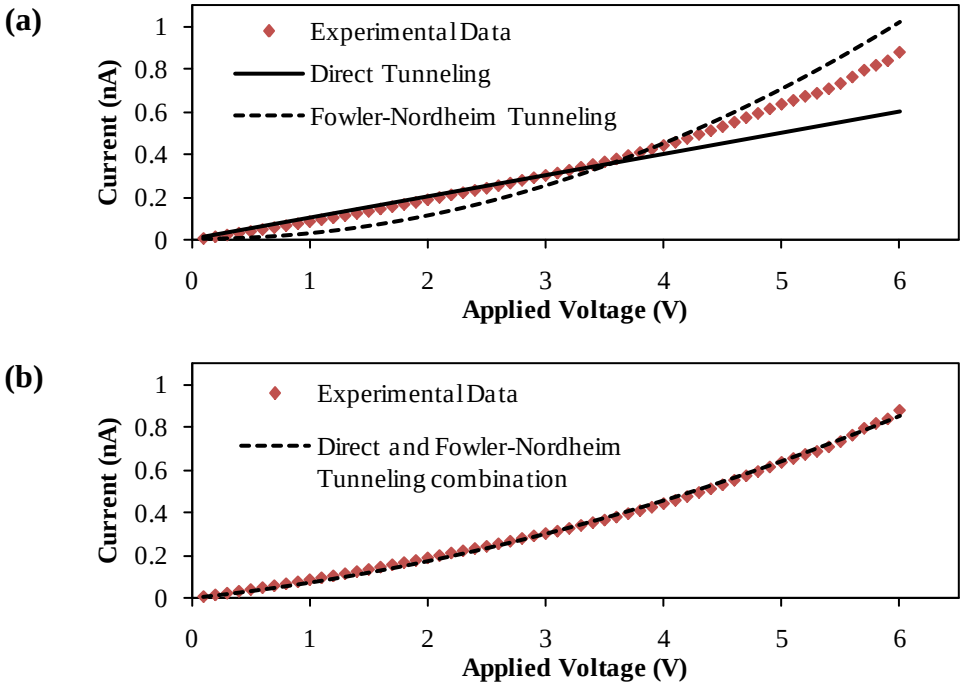


Figure 5.57(a) *I-V* characteristic of break junction with 4 mg·ml^{-1} nanoparticles showing fittings for direct tunneling and Fowler-Nordheim tunneling. (b) Same experimental data showing fit for a combination of direct tunneling and Fowler-Nordheim tunneling.

In order to confirm that the solvent used for dispersing the materials was not responsible for any of the electrical characteristics, nanoparticle devices were also prepared using both

chloroform and dichlorobenzene with a nanoparticle concentration of 4 mg·ml^{-1}. Characteristics were found to be almost identical for toluene and chloroform with only slight difference found when dichlorobenzene was used (Figure 5.58(a)). This difference could be due to the nanoparticles not dispersing in dichlorobenzene as thoroughly, resulting in a lower quality deposition. These differences were minor and it is possible to conclude that the solvent used does not significantly affect the *I-V* curves measured.

Another possible influence to the characteristics could come from the substrate material used. In all cases a 100 nm thick thermal oxide layer was grown on p-type silicon. This should offer a high quality insulating layer and ensure that there is no possibility of conduction through the silicon, however, as the oxide was grown in university facilities at the Emerging Technologies Research Centre (EMTERC), at De Montfort University [165] there is the possibility that it could include impurities and defects which would lower its quality. To confirm that the silicon was not playing a role in any of the characteristics, break junctions were also fabricated on both glass and sapphire substrates, which are both good electrical insulators. From Figure 5.58(b) the characteristics for SiO_2 and sapphire substrates are identical, showing that a breakdown of the SiO_2 layer and conduction through the silicon is not responsible for any of the characteristics.

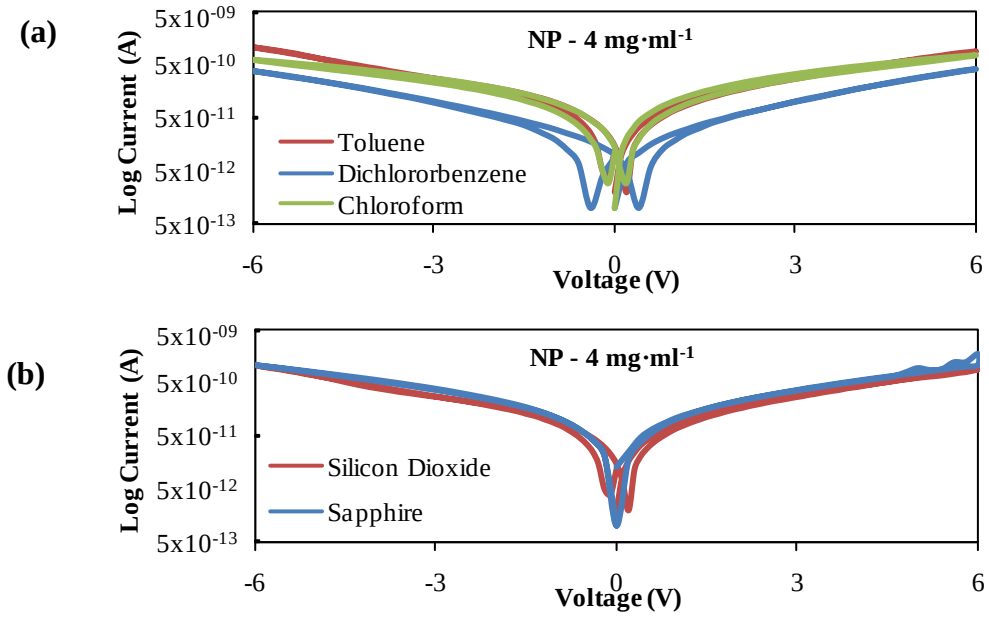


Figure 5.58 Effect on *I-V* characteristics due to change in: (a) Solvent and (b) Substrate material.

It was found that it was not possible to fabricate high quality break junctions on the glass substrates, and so no reliable measurements could be taken. Under optical magnification the gold electrodes on glass showed evidence of melting rather than the fracture formation which

characterised break junction formation on SiO_2 and sapphire. This is likely due to the low thermal conductivity of glass, which results in the electrodes melting due to the high current densities.

5.5. Summary of Chapter 5

This section has focused on the possible mechanisms that have been proposed for the change in conductivity in PMDs.

The possibility that the polystyrene itself could be either wholly, or partly responsible for the switching behaviour has been discussed and related back to experimental work conducted in Chapter 4. This mechanism has been discounted as a likely means of switching in these memories.

Mechanisms involving the charging of nanoparticles are also prevalent in literature, hence various techniques have been investigated in order to answer some of the many unknowns surrounding both the previous work conducted by other researchers, and the mechanisms and characteristics of gold nanoparticle charging in general. It was initially speculated that Coulomb blockade may be observed in the STM experiments. However, after attempts with Type-I gold nanoparticles this proved not to be the case. Tunneling currents between the STM tip and the nanoparticles were seen, yet after analysis of the curves, no evidence of a Coulomb staircase and hence no evidence of nanoparticle charging was observed.

EFM measurements were also conducted on several different configurations of nanoparticles. It was found that when the nanoparticles were embedded in a polymer matrix, as is the case for a PMD structure, then a strong EFM response could be obtained. However, experimental results on the polymer layers alone were also found to show EFM responses under charging conditions, which proves that this technique is not suitable for using as a proof of nanoparticle charging. Significantly, this technique is one of those employed by Ouyang *et al.* [9-10] as evidence to support the claim that a charge transfer between 8HQ and gold nanoparticles was responsible for the change in conductivity of their devices. By showing that this experimental setup was flawed also casts some doubt over the charge transfer mechanism being responsible for the switching in Ouyang *et al.'s* devices.

In order to eliminate any possible role of the polymer matrix material, EFM experiments on LB deposited gold nanoparticles were subsequently attempted. This proved unsuccessful due to problems of applying an electrical bias to the nanoparticles without significant damage to the LB layer. This problem was later eliminated by depositing the nanoparticles between

metal electrodes. This approach enabled the nanoparticles to be biased without having to use the EFM tip itself as the top electrode. A further benefit of this configuration was the ability to continuously capture EFM data while voltage biases were being applied, enabling the immediate effects of voltage biases to be observed, while also eliminating the possibility of the nanoparticles discharging in the time taken to change EFM probes.

Gold nanoparticle charging was also investigated using techniques based purely on electronic circuitry by depositing the gold nanoparticles between metal electrodes and measuring the response of the resultant RC circuits. With the oscilloscope used it was possible to measure sub-nanosecond response times, allowing the anticipated small increases in capacitance due to the nanoparticles and fast charge/discharge times to be accurately measured. Small changes in capacitance were detected when the nanoparticles were present, but it was not possible to confirm that this change was as a result of charging of the nanoparticles. In this case it was also possible that the increase in capacitance in the circuits could be due to the deposited nanoparticles effectively increasing the area of the electrodes, hence increasing the parasitic capacitances.

Nanoparticle charging was also investigated using MIS capacitor structures. MIS capacitors can be very sensitive to levels of trapped charge that are present in the insulating layer; a property that was initially exploited in the characterisation of polystyrene in Chapter 4. By deliberately introducing nanoparticles into the capacitors at the semiconductor-insulator boundary, hysteresis was introduced into the *C-V* characteristics which could be directly attributed to the charging and discharging of the gold nanoparticles. Other possibly sources of trapped charge such as mobile, insulator and interface trapped charges were shown to not be responsible for the hysteresis in these devices. It was also found that a relatively small number of the nanoparticles appear to be contributing towards the levels of trapped charge, indicating that charging may be confined to defect areas in the device where local distortions of the electric field result in field enhancement effects.

The magnitudes of reported current in many published works on PMDs have been investigated here by fabricating lateral nanoscale break junction electrode structures and depositing the various constituent materials of PMDs between them. Even in devices consisting purely of nanoparticles, the measured levels of current found here were several orders of magnitude lower than those that are regularly reported for the *on* state current in PMDs. This casts serious doubts over the mechanism of tunneling between nanoparticles, or any other constituent material being responsible for the high current levels in the *on* state

characteristics of nanoparticle PMDs. By fitting theoretical equations to experimental data it has also been shown that some of the justifications used by Ouyang *et al.* [9] and Yang *et al.* [14] for the conduction mechanisms in PMDs are flawed, and that several different conduction mechanisms could be made to fit the experimental data.

Importantly, in the lateral PMDs that were fabricated with the break junctions as electrodes, there was no evidence of switching between two memory states. If the mechanism of switching was due to nanoparticle charging, then lateral PMDs would be expected to switch in much the same way as vertical device structures. Even accounting for the reduced device area of the lateral PMDs, some evidence of hysteresis or switching would have been expected. Experimental characteristics of the lateral PMDs and also of many of the constituent materials were found to closely resemble in shape the *on* state characteristics reported in many PMDs. The lack of switching, and the shape of the *I-V* characteristics suggests that the *on* state current levels in some PMDs are actually the normal conductivity level of nanoparticle loaded polymer layers. This implies that there may be some other mechanism that is responsible for the low *off* state current in PMDs. This concept will be discussed further in §6.2.

Investigations were carried out to study the feasibility of filamentary formation occurring in PMDs. The theoretical required density of filamentary material was calculated and found to be relatively low at one filament per 9.25 μm^2, based on 1 nm diameter filaments. Temperature rise during evaporation of top electrodes showed that significant temperatures can be obtained if slow evaporation rates are used, which could lead to damage at the polymer/metal boundary and penetration of metal into the polymer. Further evidence of metal penetration comes from the lack of viable MIM devices fabricated with gold and chromium electrodes. Many of these devices showed ohmic *I-V* characteristics which suggest that these metals can readily penetrate through several tens of nanometres of polymer.

Filamentary switching has also been demonstrated in break junction devices. These structures showed repeatable switching behaviour in their as fabricated state, before the addition of test materials between the electrodes. This immediately rules out the possibility of the test material being responsible for the switching. The characteristics were stable over multiple *write* and *erase* cycles and showed an increase in current of six orders of magnitude in the *on* state. Metallic conduction was confirmed by the ohmic characteristics of the devices in the *on* state.

Damaged areas of PMDs were investigated, with considerable damage to both the top electrode and the underlying polymer layer becoming present at voltages significantly lower than would be expected for dielectric breakdown. This damage was shown to extend down to the bottom electrode and could highlight areas where filaments may have been present. Field enhancement effects between nanoparticles in the devices and also between defects and pinholes are likely, with electric field simulations showing field enhancement factors of >2 are possible. This explains the damage and dielectric breakdown that is occurring at lower than expected voltages and shows that significant damage can occur at relatively low voltages.

CHAPTER 6

Required Characteristics and Realisation of Functional Memory Devices

In this chapter there follows discussions concerning the characteristics that are required for memory devices designed for differing applications, along with more general design considerations. Control and interface circuitry for use with PMDs will also be described, showing the viability of simple circuitry being used for the control and decoding of multiple memory cells in parallel.

The experimental characteristics of gold nanoparticle based MIM memories are shown along with a discussion of the theorised working mechanisms responsible for the conductivity change for S, N and O-shaped memory characteristics.

Memory devices based around an MIS structure are then demonstrated, with the features of these devices discussed and compared to MIM structures.

6.1. Required Characteristics of Nanoparticle PMD

At its most fundamental level a rewritable non-volatile memory is required to retain two memory states when no power is applied. It must also be able to *erase* and *write* data when needed. The exact requirements in each of these fields are then dependent upon the required application of the memories. By considering a PMD that can exist in one of two conductance states, defined as *1* or *0*, the *on/off* ratio is generally used to demonstrate the PMDs bistability. However, as has also been argued by Scott *et al*. [166] there has been a tendency in many research papers to overemphasise the benefits of having a large *on/off* ratio, with this characteristic usually being used as the main selling point of any new devices. While it is true that having a large *on/off* ratio can be beneficial, in reality the variability between different devices in a memory array, and even the variability in a single device over several switching cycles is a much more important characteristic. Consider the following:

1. An array of PMDs with a large *on/off* ratio of 10^5, but also a large variability in device characteristics (Figure 6.1(a))
2. An array of PMDs with a low *on/off* ratio of 100, but a very tight variation in device characteristics. (Figure 6.1(b))

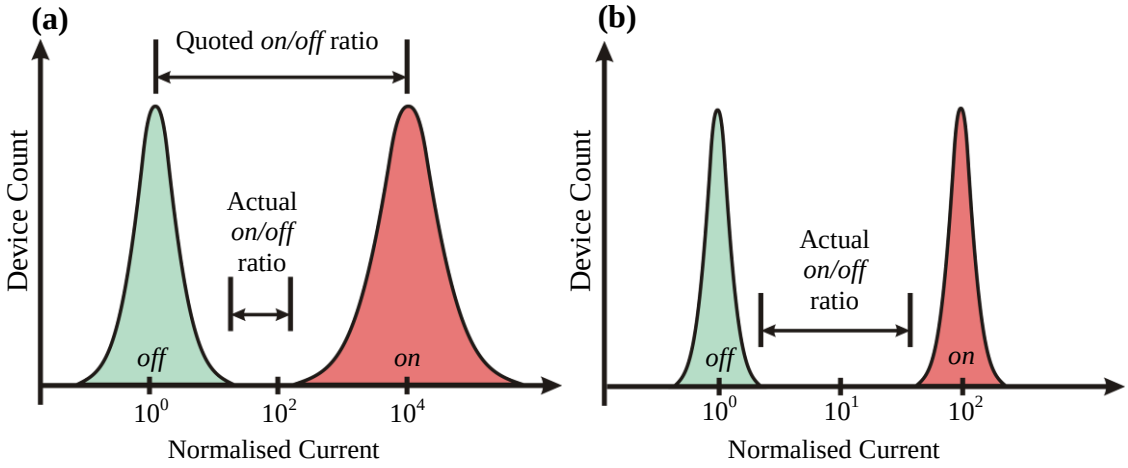


Figure 6.1 Device variability considerations. (a) Large variability. (b) Low variability.

By carefully designing the associated circuitry that decodes the state of the PMDs, so that it has the ability to differentiate between *on* and *off* states that may be quite close, the second set of devices are actually favoured, as these will prove to be more reliable when reading the data. This also highlights a major problem in published research, that quoted *on/off* ratios are largely between a single device. For a practical memory the *on/off* ratio needs to be the difference between the maximum spreads of the two states, as illustrated in Figure 6.1(a).

If two scenarios are considered then it is possible to estimate the minimum required specifications for memories, as shown in Table 6.1. The first scenario is that PMDs will replace all current memory technologies as in the vision outlined by Scott [3], and in the second that PMDs will simply offer ultra-low cost memories for less demanding applications. Possible foreseeable applications could include disposable electronics, or flexible electronics such as electronic newspapers. In the example of an electronic newspaper a few megabytes of memory would likely suffice, with the data being written on a daily basis for the duration of a one year subscription to a service.

Table 6.1. Minimum requirement for a PMD under different scenarios.

Characteristic	Universal Memory	Electronic newspaper
Retention time	> 10 years	1 week
Memory cycles	$> 10^{15}$	~1000
Read/write/erase speed	$\sim 10^{-9}$ seconds	$< 10^{-7}$ seconds (based on writing a 5 Mb file in 15 seconds).

As discussed the *on/off* ratio is very much linked to the device variability, but circuitry can readily be designed to accommodate ratios as low as 10, as is shown in §6.4. Requirements such as power consumption would have to be comparable with today's technologies and would become an important characteristic for battery power applications such as the newspaper. In terms of memory density, for a universal device this would likely have to scale down to nanometre dimensions in order to compete with current memories. This has been shown to be possible for single devices where Paul *et al*. [101] demonstrated bistability at nanoscale dimensions, however the practical implications of making connections to a cross-point array this dense could prove problematic. For the low cost application a 5 Mb memory in a 1 cm^2 area is realistic, meaning the cell size would be in the order of 1 μm^2. Another inherent drawback of a resistive cross-point array of memory cells here becomes apparent, with the problem of accessing a single cell (or row of cells) without all the cells in the array responding to the *read* voltage. This problem was also highlighted by Scott *et al*. [166] who proposed the solution of either having to make the memory elements themselves rectifying, or introduce a diode into each memory cell. This problem is demonstrated in Figure 6.2(a) and (b). Without any rectification, current in an array of resistors will always flow through the path with the least resistance. In this case a high *on/off* ratio is actually detrimental, as the *on* state resistance will also be many orders of magnitude lower, meaning the current contribution from leakage paths will dominate in the array. In reality whether an array is viable or not depends upon the position in the array of the *on* cells, but it could be possible to short circuit an entire array where each row and column had only two cells in the high conductivity state.

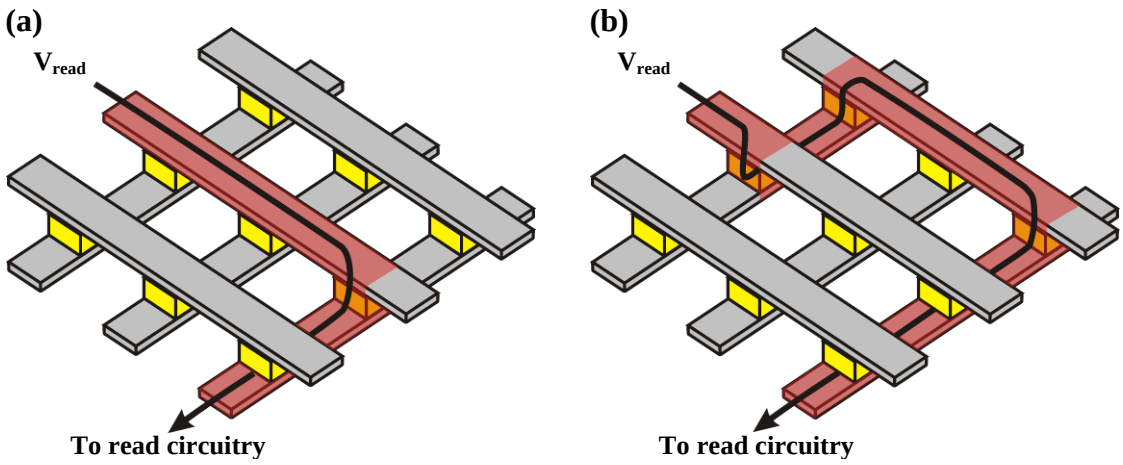


Figure 6.2(a) Desired reading of a PMD cell. (b) Unwanted read pathways through the array.

6.1.1. Experimental *I-V* Characteristics of Nanoparticle Containing Metal-Insulator-Metal Polymer Memory Devices.

Polymer memory devices were fabricated to the same specifications as those studied by Ouyang *et al*. [9]. Polystyrene (PS), 8-Hydroxyquinoline (8HQ) and Type-I gold nanoparticles (NP) were used at concentration of 12 $mg \cdot ml^{-1}$ PS and 4 $mg \cdot ml^{-1}$ 8HQ and nanoparticles (termed 4-NP+8HQ+PS devices), with dichlorobenzene as the solvent. Admixture layers approximately 50 nm thick were spin-coated onto bottom aluminium electrodes, with the top electrode evaporated at greater than 1 $nm \cdot s^{-1}$ to minimise any temperature rise. To compare the effects of the constituents, devices were also fabricated with only the 8HQ and polystyrene (8HQ+PS devices) in the active polymer layer and also with nanoparticles and 8HQ at concentrations of 8 $mg \cdot ml^{-1}$ (8-NP+8HQ+PS devices) and 12 $mg \cdot ml^{-1}$ (12-NP+8HQ+PS devices).

6.1.2. Characteristics of 4-NP+8HQ+PS devices

Initial *I-V* characteristics of these devices were measured in order to ascertain the memory characteristics and setpoint voltages required for the *read*, *write* and *erase* potentials. Due to the similarity in device structure between the devices manufactured here and those that are prevalent in literature it was expected that some form of abrupt switching may occur, with the possibility of NDR also being present. However, as shown in Figure 6.3 only hysteresis occurred in these devices leading to O-shaped characteristics. In order for the hysteresis to become apparent the devices also had to undergo several *I-V* cycles indicating that there is a conditioning period needed before full hysteresis is observed. Similar conditioning periods have been common in most polymer MIM structures that have been investigated during this study, which indicates the conditioning period in the PMDs is due to the polymer matrix rather than any influence of the nanoparticles or 8HQ.

It was found in these devices that breakdown voltages were significantly lower than would be expected for the case of polystyrene alone as the dielectric, with damage appearing on the top electrode and breakdown in the *I-V* characteristics between voltages of 6 – 10 V. This results in a breakdown field strength of 1.2 – 2 $MV \cdot cm^{-1}$, less than half the expected breakdown strength found for polystyrene in §4.3.1, this would be consistent with the field enhancement factor of 2, which was found to be possible in §5.3 by introducing nanoparticles into the dielectric.

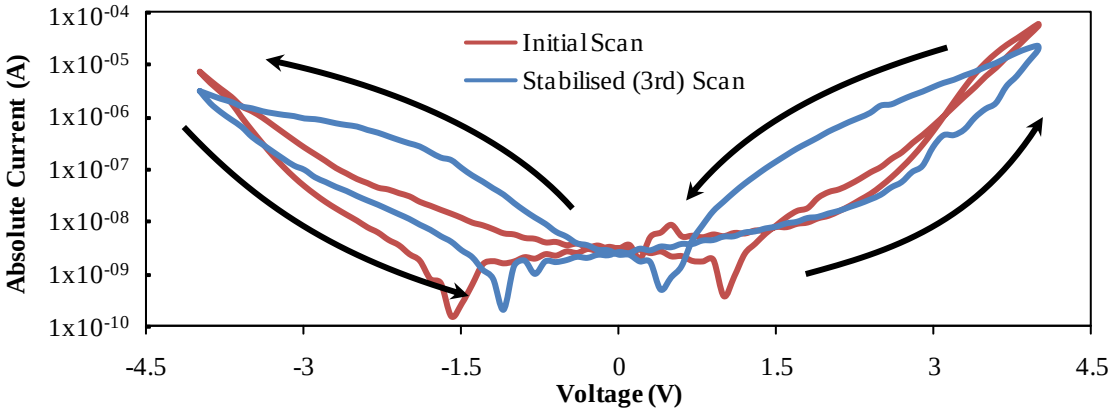


Figure 6.3 Initial and stabilised *I-V* characteristics of a 4-NP+8HQ+PS PMD. Arrows indicate direction of hysteresis, voltage scan rate = 0.1 V·s^{-1}.

To confirm that the hysteresis is as a direct result of introducing nanoparticles into the devices Figure 6.4 shows the comparison between the *I-V* curves for PS only devices, and devices with 8HQ and nanoparticles.

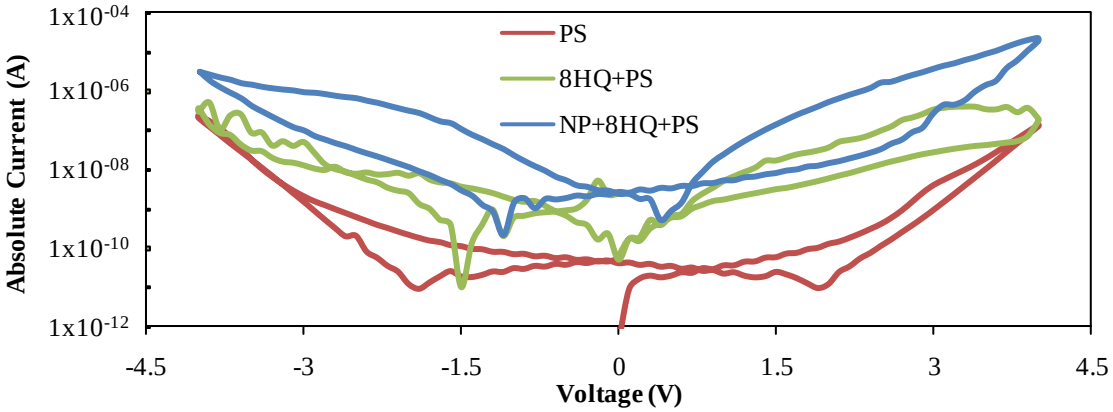


Figure 6.4 Comparison of *I-V* characteristics for different active layer compositions. Voltage scan rate = 0.1 V·s^{-1}

These characteristics were taken after several cycles and can be considered to be the conditioned characteristics. It can be seen that only the devices with gold nanoparticles result in useful magnitudes of hysteresis. The devices with 8HQ did show a small amount of hysteresis, but the curves proved to be unreliable, with an appreciable amount of noise present.

The *I-V* characteristics show that bistability is possible in these devices, but to characterise the longer term performance of the memories both *read*, *write* and *erase* cycles, as well as retention time experiments have to be carried out. Due to the conditioning period that is needed in these devices, the initial cycles show a gradual increase in the hysteresis

amounts and hence the memory window, with the *on* and *off* state currents as a function of the cycle number shown in Figure 6.5(a). It can also be seen that after a period of operation lasting approximately 60 cycles, the memories failed, with a significant drop in the levels of both current and hysteresis.

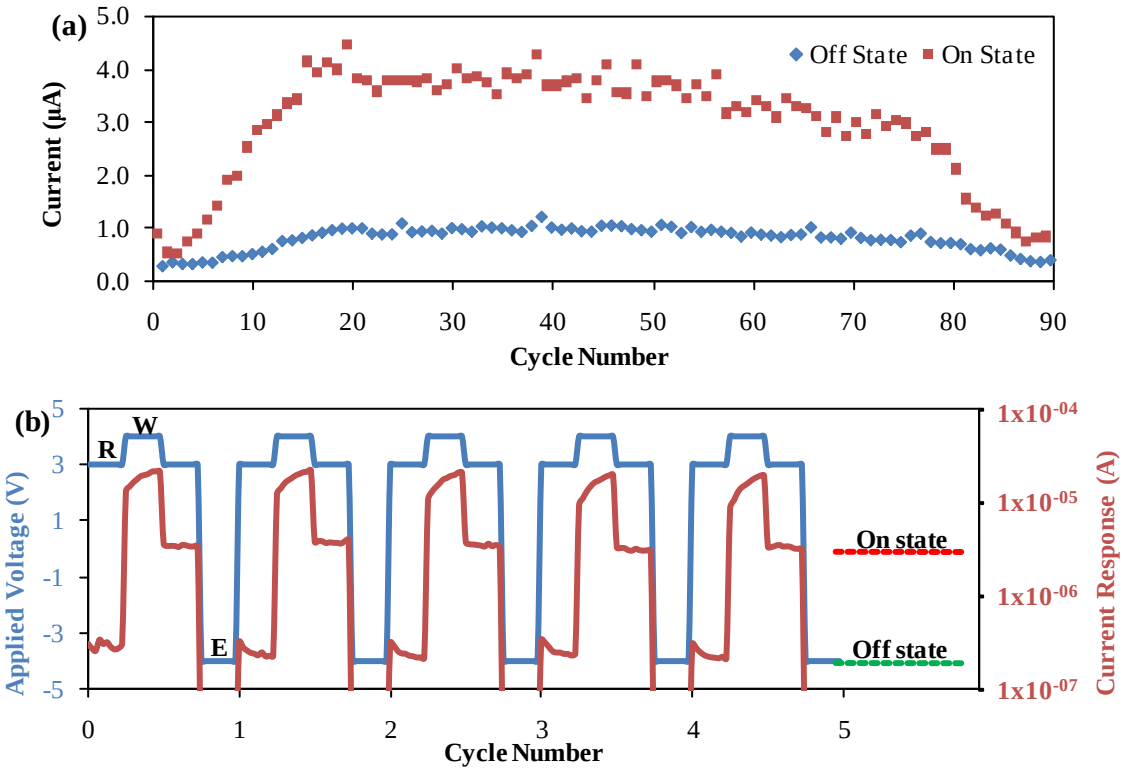


Figure 6.5(a) *On* and *Off* currents as a function of the RWE cycle number. (b) Selected *read*, *write* and *erase* cycles for 4-NP+8HQ+PS PMD.

This behaviour was found to be typical for all the memories measured, with the maximum hysteresis at approximately the 20th cycle, and all memories failing between 60 – 90 cycles. Figure 6.5(b) shows the actual RWE cycles over a five cycle period, showing an *on/off* current ratio of ~10. This was found to be typical for these devices with average *on* and *off* currents of 4.8×10^{-6} and 2.9×10^{-7} amperes respectively, however, while the *off* state currents were found to have a narrow current distribution (standard deviation = 1.2×10^{-7} A), the *on* state currents showed a large degree of variability with a standard deviation of 2.4×10^{-6} A. The extent of this variation means that in reality these devices could not be used reliably as memory devices, as there is a significant overlap in the distributions of the currents.

Typical retention time characteristics of these devices are presented in Figure 6.6, showing 10,000 *read* pulses over a period of three hours. A *read* voltage of 3 V was used after applying *write* and *erase* voltages of ±4 V. Over this time period the two states

remained stable, with a gradual decay in the *on* state current evident, resulting in the initial *on/off* current ratio of ~20 decaying to a ratio of ~8 after three hours. However, the ratio decayed below 10 after approximately 1.5 hours, highlighting that in these devices retention time requirements are not met for even low specification disposable electronic applications (see Table 6.1).

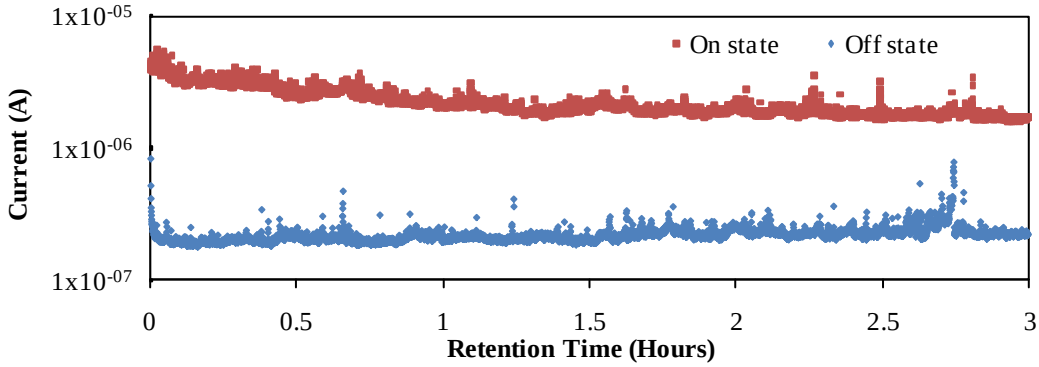


Figure 6.6 Retention time of a typical 4-NP+8HQ+PS PMD.

The retention time characteristics can also provide information about the mechanisms that are responsible for the hysteresis and memory characteristics of these devices, with the gradual decay in current being an indication that a charging phenomenon may be responsible for the change in conductivity of the devices. Further information can be found from looking at the *I-V* curves in the *on* state of the devices, and investigating the possible conduction mechanisms present. By plotting the log of the current density vs. square root of the voltage it is evident that this provides a good straight line fit. This would also be the case if current density/voltage vs. square root of the voltage were plotted indicating the conduction mechanism is either Schottky or Poole-Frenkel emission (Figure 6.7(a)). As discussed in §4.3.2 to distinguish between the two mechanisms symmetry, or asymmetry in the *I-V* characteristics needs to be investigated. From the *I-V* curves shown in Figure 6.7(b), there is asymmetry between the positive and negative voltage scans, which suggests Schottky emission is the dominant conduction mechanism, with the current being electrode limited.

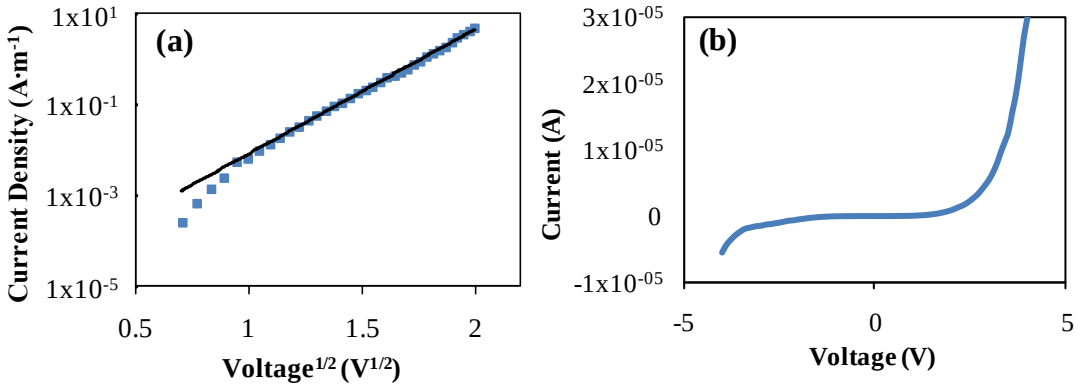


Figure 6.7(a) Dependence of the current on the square root of the voltage in the on state. (b) Asymmetry in the *I-V* characteristic of a 4-NP+8HQ+PS PMD.

As both top and bottom electrodes were aluminium, this asymmetry would not normally be expected, as the barrier heights should be identical. This leads to two possibilities that could give rise to asymmetrical behaviour, either metal penetration from the top electrode could alter the metal-insulator interface, or a thin native layer of aluminium oxide could be present on the bottom electrode before the polymer layer is spin-coated. Similar asymmetry was also present in the devices with only polystyrene as the insulator, suggesting all the devices fabricated at the same time had this asymmetry in barrier heights.

This conduction mechanism suggests that the electrodes are playing an important role in the memories, however they are not responsible for the hysteresis itself, as, if this were the case, then the devices without nanoparticles would also have been expected to show hysteresis. The fact that hysteresis is present, and that the *on* state current shows a steady decay over time, suggests that in these devices charge storage on the gold nanoparticles is responsible for the memory effect.

Subsequent attempts to fabricate devices to the same specifications, but with Type-II gold nanoparticles resulted in devices showing no hysteresis and no memory effect. This highlights the problem that the memory effect appears to be very dependent on the fabrication conditions and material selections, with small changes in device structure leading to unviable devices. The reproducibility in these devices is a major problem for their future use as memory devices. Only one substrate of viable devices was fabricated, with 16 out of 20 devices showing reproducible switching. However, only six of these had distributions in their currents tight enough to be able to reliably operate when used in conjunction with each other.

6.1.3. Nanoparticle Concentration Effect on Memory Characteristics

Due to the lack of sudden switching in these devices, as has been reported in many PMDs, devices with a nanoparticle and 8HQ concentrations of 8 and 12 $mg \cdot ml^{-1}$ were fabricated in order to ascertain whether higher levels of nanoparticles would lead to switching behaviour or short circuiting of the devices. It was found that in all cases the 12-NP+8HQ+PS devices had very low breakdown voltages with devices short circuiting at under 2 V. After breakdown these devices showed ohmic characteristics, with resistances in the range of 20 – 850 Ω, indicating that metallic material bridging the electrodes was responsible for the breakdown, rather than tunneling through a percolated network of nanoparticles.

At concentrations of 8 $mg \cdot ml^{-1}$ the majority of devices also short circuited at low voltages of between 2 – 3 V, however there were small numbers (2 out of 16 devices) which showed a single switching characteristic to a higher conductivity state (Figure 6.8). There was no reversible switching in these devices, with only WORM characteristics found.

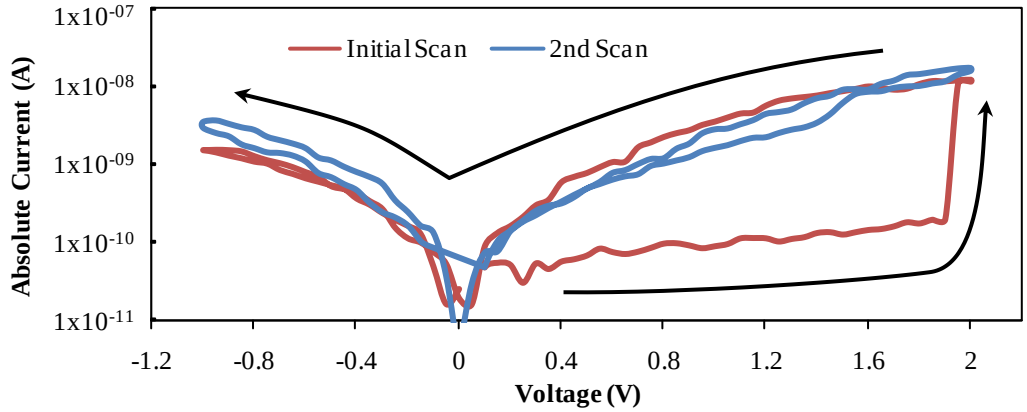


Figure 6.8 *I-V* characteristics for an 8-NP+8HQ+PS PMD. Arrows indicate direction of hysteresis.

The *on* state *I-V* characteristics in these devices were once again found to fit well with either Schottky or Poole-Frenkel emission, with asymmetry in the curves indicating Schottky to be the most likely. The sudden switch to this conductivity state could be an indication that dielectric breakdown is occurring in an aluminium oxide layer on the bottom electrode, thereby switching to the normal conductivity mechanism through the polymer. A lack of hysteresis in these devices indicates that no charging took place. This may be due to the lower voltages of operation used, with higher voltages resulting in breakdown of the devices. The lack of charging is also evident in the retention time characteristics of these memories, as shown in Figure 6.9.

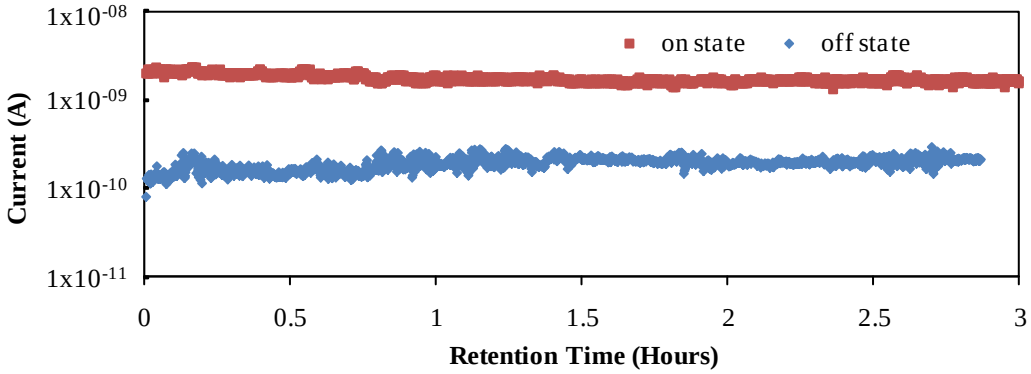


Figure 6.9 Retention characteristics of an 8-NP+8HQ+PS PMD.

If charging were taking place then the current level in the *on* state would be expected to decay with time, as the charge is dissipated, however, with these devices the current in the two states is very stable, with no evident drop in the current levels over a period of 3 hours.

6.2. Summary of Memory Mechanisms in Metal-Insulator-Metal Polymer Memory Devices

As previously discussed the characteristics that have been reported in PMDs can be separated into three broad categories; N-shaped, S-shaped and O-shaped. It was hypothesised that these different characteristics would likely have different mechanisms that were responsible for the change in conductivity of each. From the experimental data gathered during the course of this investigation, there is strong evidence to suggest that this is indeed the case.

6.2.1. S-Shaped Characteristics

Two types of mechanisms seem to be responsible in this case dependent on the current levels and the conduction mechanisms that are present in the *on* state of the devices. In §5.3 it was shown that the maximum current that a nanoparticle filled polystyrene film could support was in the range of tens to possibly hundreds of nanoamperes, at thicknesses of approximately 20 – 40 nm. Higher currents may be possible if other polymer materials are used, for instance if semiconducting polymers were used then higher currents may be expected before damage to the polymer occurs. However, for devices where very high *on* state currents are reported (several microamperes and milliamperes), it is unlikely that this level of current can be supported by the polymer material alone. This is especially true where

characteristics are ohmic, or near to ohmic and it is likely that a breakdown mechanism is responsible here, with conduction through localised conductive areas.

For lower levels of *on* state current, which the break junction experiments showed could be supported by the nanoparticle loaded polymer layer, another mechanism is suggested. The break junction data was collected from devices where electrode influence on the characteristics was minimised, guaranteeing that there was no oxide formation, or influence from an evaporated top contact. In these break junction devices the *I-V* characteristics very closely resemble the *on* state *I-V* curves for published PMDs, which suggest that it is not the charging of the nanoparticles that is responsible for the high conductivity state, but that this level of conductivity is the normal level for nanoparticle/polymer admixtures. In this case the *off* state in the devices would then be due to current being blocked by influences from the evaporated electrodes, possibly from a thin native oxide layer on the bottom electrode. As initially discussed in §2.3.2, switching in oxide films has been studied for in excess of 40 years, and while it may still not be fully understood, it has been shown to be reversible and able to undergo many switching cycles. It is proposed that in many of the S-shaped devices the oxide layer is present and intact in the as fabricated state, resulting in the initial *off* state characteristics. At a certain threshold voltage this oxide layer can switch which results in a sudden increase in current to the normal conductivity level for the nanoparticle loaded polymer. The low conductivity state can then be returned when the oxide film is switched back to its *off* state. This would explain why devices are in the *off* state when fabricated, as discussed by Bozano *et al*. [12]. Some of the models based on charge trapping and space-charge inhibition of injected current would suggest that the device should initially be in the *on* state before any charge is trapped.

The fact that nanoparticles/nanocrystals are required for switching is also explained, in so far as the normal conductivity level of the polymer has to be significantly higher than conductivity in the *off* state. If the polymer matrix is insulating, then the inclusion of nanoparticles increases the conductivity level to one where a noticeable *on/off* ratio is observed. For the case of semiconducting polymers the nanoparticles may not be needed, as the polymer itself is already conductive enough [86]. This does however suggest that with the correct choice of polymer the need for nanoparticles is dispensed with. The simplest structure would then be one where a high conductivity polymer is used initially, however, if for material property reasons an insulating polymer is more suitable, then any material which would make the polymer more conductive could be added.

Finally this mechanism also explains why there are many different conduction mechanisms quoted in literature. Conduction mechanisms are dependent on the materials used and the exact compositions of the devices studied, so depending on device structure and materials, the exact ratios of constituents used, or even the research group that is making the device, it is quite possible that range of different conduction mechanisms would be applicable.

6.2.2. O-Shaped Characteristics

In these devices no sudden switching was evident, and also the *on* state characteristics showed no evidence of ohmic behaviour, indicating that a breakdown mechanism in the polymer or filamentary conduction was not responsible for the change in conductivity. The simple hysteresis in the characteristics and the low retention times, with a gradual decrease in the *on* state current of the devices when subjected to multiple, consecutive *read* pulses, suggest that a charging mechanism is more likely to be responsible in these devices. There are still unanswered questions remaining concerning the exact role of the electrodes in the devices though, with the *on* state current being electrode limited Schottky emission. This shows that the electrodes play an important role in the current conduction, and could also play a role in the switching and hysteresis behaviour too.

Also there was the issue of high current levels through these devices, with *on* state current of ~5 μA at relatively low voltages of 3 V. From the break junction devices current levels of this magnitude should not be possible in undamaged polymer layers containing only polystyrene, gold nanoparticles and 8-hydroxyquinoline, which would suggest that those PMDs showing hysteresis were defective in some way, resulting in much higher conductivity than would be expected. All the devices fabricated in the same batch (devices with PS, 8HQ+PS and NP+8HQ+PS as the active layer) showed higher than expected conductivities. The common elements in all the devices were the polystyrene solution and the evaporation of the aluminium electrodes, which would imply that there may have been some contamination of the polystyrene solution itself, or contamination/damage from the top electrode that altered the properties of all the devices. This would explain why the results were irreproducible, with only one batch of devices showing reproducible hysteresis, while subsequent attempts to fabricated PMDs with O-shaped characteristics failed. It doesn't however explain why only devices with nanoparticles showed reproducible hysteresis, unless a combination of

nanoparticle charging and/or contamination and/or electrode effects were responsible. Unless these results can be replicated in the future, the exact mechanisms will remain speculative.

6.2.3. N-Shaped Characteristics

During the course of this investigation none of the devices, or test structures fabricated showed N-shaped characteristics, hence there was no evidence of NDR. For this reason only brief comments can be made about possible switching mechanisms in these devices, as there is a lack of experimental data with which to substantiate any theories. The most recent theories that have been proposed to explain the NDR that is present in N-shaped characteristics are firstly the formation of a space charge field which inhibits the injection of carriers, leading to a reduction in current and hence the NDR effect [167]. The second theory is due to filament formation, which will start to rupture at certain current densities, resulting in a lower filament density and lower current levels. Both theories do appear to offer an overall explanation of the shape of the curves, but on closer examination, filamentary conduction in this case seems the less likely. Firstly, in the gold break junction experiments conducted in §5.3, the switching that could be attributed to filament formation resulted in S-shaped characteristics. Similar characteristics were also found by Baek *et al.* [162] where the switching showed a high likelihood of being filamentary, indicating that the filaments may not rupture at higher applied voltages. Secondly, filament formation would be expected to result in ohmic, or near ohmic conduction in the *on* state, which is not the case when *on* state characteristics are reported [12, 94, 160].

This may indicate that filamentary formation is not the responsible mechanism for many of the devices that show NDR, and that the formation of a space charge field could be possible. However, with this mechanism there are still some problems that remain unanswered, such as why the devices are in the *off* state when fabricated, as the device would be expected to have no space charge field in this case and hence be in the *on* state.

6.3. Experimental *I-V* Characteristics of Nanoparticle Containing Metal-Insulator-Semiconductor Polymer Memory Devices

For any memory device to be reliably used in a commercial application the mechanisms of operation will have to be proved beyond doubt, and proved to be reliable for the duration of the memories expected lifespan. Currently this is not possible with PMDs based on an MIM structure, for the reasons highlighted in the previous sections. Another structure that

offers the possibility of being used as a memory device is the MIS structure that was extensively used in §4.5 and §5.2.6. This structure has been extensively studied and is known to be highly sensitive to the levels of trapped charge present in the insulating material, especially if that charge is present at the boundary between the semiconductor and the insulator [111]. This principal was exploited in §5.2.6 to show that gold nanoparticles could be charged and to estimate the levels of charge that could be trapped, however, these devices also show the basic hysteresis requirements needed to function directly as memory devices themselves. For example in Figure 6.11(a) if the capacitance measured at -1 V is taken, then depending upon whether a high, or low voltage pulse has just been applied, the capacitance can either be in a high or low state. This shift in the *C-V* curves can be explained by considering how the introduction of nanoparticles at the silicon-insulator interface affects the depletion width in the silicon under different gate voltage conditions. For charge neutrality in the devices, when a voltage is applied to the gate electrode, this has to be balanced by an equal and opposite charge in the insulator or the silicon. In an ideal device this charge is always provided by the silicon, as illustrated in Figure 6.10(a), however, when a layer of trapped charge is present this will provide a portion of the compensating charge. This leads to a reduction in the amount of charge provided by the silicon, a reduction in the depletion width, and hence an increase in the capacitance at any given voltage resulting in a shift in the *C-V* curve along the voltage axis.

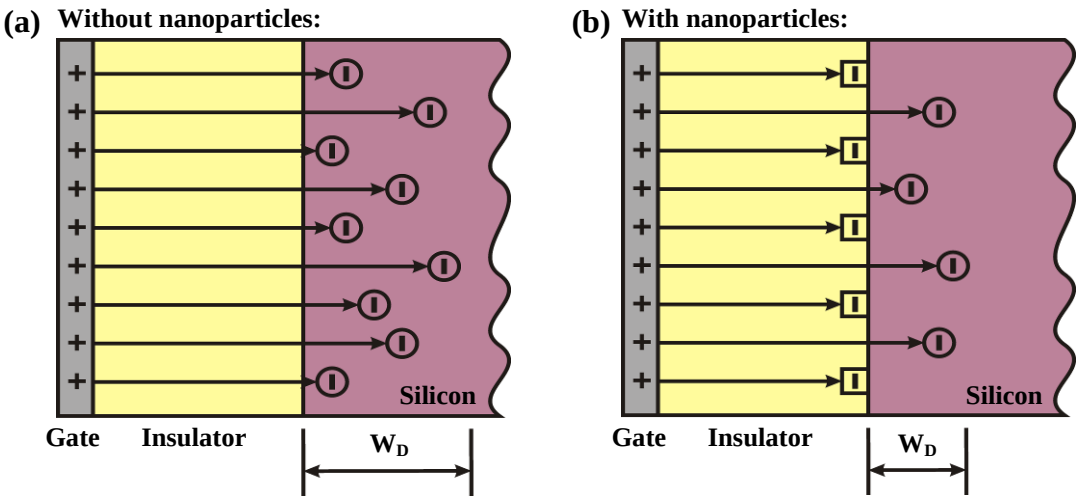


Figure 6.10(a) Compensating charge when no insulator trapped charge is present. (b) Insulator trapped charge due to nanoparticles partially screening the applied gate voltage.

As this charge is provided by nanoparticles which have been shown to be capable of reliably charging and discharging, this resultant hysteresis is tuneable dependent on whether a *write* or *erase* voltage has previously been applied to the gate.

MIS capacitor structures have previously been used as the basis of memory devices. However, their use is often with the intention of integration in to transistor structures and is more akin to flash memory [87, 168-169]. Other uses have included showing hysteresis characteristics to illustrate that charge storage is possible in trap sites that have been introduced into the insulator [88, 156], or with the intention to be used directly as memories, but with only basic characteristics and retention times reported [170].

MIS structures were fabricated to the same specifications as those used in §5.2.6. As it was previously found that incorporating several layers of nanoparticles was ineffective at increasing the levels of flatband voltage shift, due to only a small percentage of the nanoparticles being charged, devices were fabricated with a single Langmuir-Blodgett monolayer of Type-II gold nanoparticles. All measurements were carried out at 1 Mhz with an alternating current (AC) bias of 150 mV. In all cases for these devices *write* and *erase* voltages of -8 V and 6 V respectively were used, with a *read* voltage of either -1 V or -0.5 V dependent on the fabrication batch.

Over multiple memory cycles the MIS based PMDs proved to be quite stable, with a typical series of RWE cycles shown in Figure 6.11(b). Each capacitor was subjected to 1000 RWE cycles, with the majority showing little degradation in performance over those cycles, as illustrated in Figure 6.11(c) which shows the *on* and *off* capacitance levels for each of the 1000 cycles. One device also had 10,000 cycles applied, once again showing little drop in performance, indicating that these memories are capable of being rewritten many thousands of times. These devices however, did show reasonably short retention times, with a significant drop in the measured *on* state capacitance over a period of approximately 2 hours. The capacitances do stabilise after this initial drop, but stabilised capacitance differences between the two states of only 5 – 10 pF were typical, which would likely prove to be too small a difference to reliably distinguish between the states when device variability is taken into account. This decay also confirms that nanoparticle charging is responsible for the hysteresis, with the devices likely to be ‘leaky’ due to the organic insulator used leading to the stored charge dissipating and a collapse of the hysteresis.

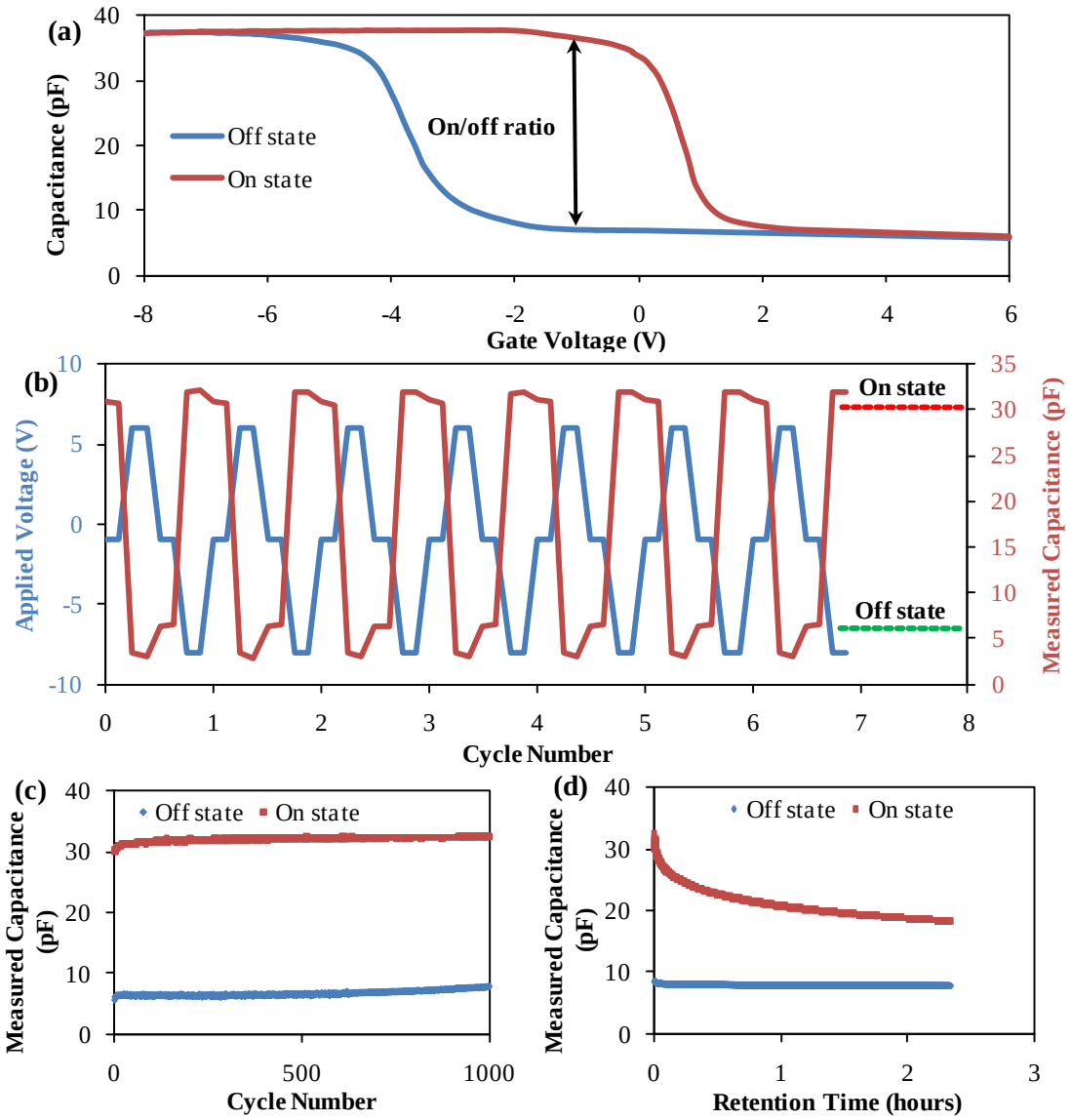


Figure 6.11(a) *I-V* characteristics of a typical MIS PMD showing a large hysteresis window. (b) RWE cycles for a typical MIS PMD. (c) Stability of *on* and *off* states over 1000 *write* and *erase* cycles. (d) Retention time of MIS PMD.

Out of 22 devices measured, all showed hysteresis windows in excess of 3 V, however, five failed to show reproducible characteristics for the duration of the 1000 RWE cycles. The remaining 17 devices showed stable characteristics throughout the RWE cycles, with an average *off* state capacitance of 10.4 pF, with a standard deviation of 4.4 pF. The average *on* state capacitance measured 32.2 pF with a standard deviation of 2.1 pF. This shows that device distribution also needs to be improved further, to ensure that overlap of distributions does not occur and measurable *on/off* ratios are maintained.

There are both advantages and disadvantages of using MIS structures as PMDs, some of which will be highlighted here with the possible consequences:

Advantages:

- Known mechanism of operation: these memories are known to operate as a direct result of charge storage at the semiconductor-insulator interface, which is as a result of deliberately introducing a gold nanoparticle layer into the memories. As it is a known mechanism, without the continued speculation that exists for MIM PMDs, the performance of these MIS PMDs can be reliably predicted, making them more attractive for commercialisation.
- The characteristics of the memories depend on the device dimensions and the materials used, hence the capacitance levels and *on/off* ratio offer some degree of flexibility for tailoring. Also smaller devices would likely lead to less distribution in the characteristics, as over smaller scales the devices should have less variability in the insulator thickness and smaller numbers of defects present.

Disadvantages:

- Connection of devices into an array could prove problematic: the silicon layer itself may need to be isolated from the silicon in surrounding devices which would increase the fabrication complexity.
- Scaling of devices: as the dimensions of each cell are reduced the capacitance will be reduced. This can be partially offset by using thinner insulating layers, but this will also be likely to effect the retention times of the devices, as the stored charge will easily leak through a thinner insulating layer. For example for a 1 μm^2 cell size and an insulator thickness of 15 nm the accumulation capacitance would be approximately 2 fF, and the inversion capacitance up to an order of magnitude less. Capacitances this low could prove problematic to reliably measure. At these capacitances the parasitic capacitances of the interconnects may also dominate, which will put limits on the speed of the memories and the minimum cell sizes achievable.
- The voltage operation of MIS PMDs is also different to that of MIM PMDs, in so far as an AC voltage is required to measure the capacitance state. This will increase the complexity of the circuitry needed for the control of the PMD, but could in fact be advantageous when it comes to reading the data. Consider the case of a typical PMD when a *read* voltage of -0.5 V DC, 150 mV AC was used. The measured capacitances were 11 pF and 31 pF for the two states, with corresponding measured AC currents of

11 µA and 30 µA respectively. This means that while the *on/off* ratios are not large, the actual currents that will be measured are larger, when compared, for instance to the current levels of the MIM PMDs in §6.1.2.

6.4. Polymer Memory Device Control and Decoder Circuits

The basic function of any memory device is the ability for it to be able to store an array of data. However, for it to be of any practical use, that data has to be accessible and interface with computer systems. Bistable behaviour has been shown to be possible in gold nanoparticle based MIM and MIS structures, proving that the concept of a PMD is possible. For any useful information to be stored in such a memory, there has to be circuitry demonstrated capable of performing all the required *read*, *write* and *erase* functions, as well as being able to decode the state of the data in the memory.

For that reason concepts have been developed for circuitry that can interface with the memory devices and provide all the necessary logic for reading from, and writing to the memories. Considerations were also made for the scalability of the circuits, with provisions made to be able to interface with PMDs up to 8 bits wide and up to 256 rows in length.

6.5. Circuit Designs for Interfacing with Polymer Memory Devices

To facilitate ease of assembly and use, the circuitry was split into four separate functional areas, each of which is assembled on its own printed circuit board (PCB):

- Voltage supplies.
- Address decoders.
- Interface board.
- Output circuitry.

Additionally due to the nature of the PMDs, they require several different voltages to be supplied depending on whether a *read*, *write* or *erase* cycle is in progress. As a result of this a combination of digital and analogue circuits need to be combined to allow correct circuit operation. This combination of integrated circuit types will be discussed in greater detail in the following sections

EAGLE (Easily Applicable Graphical Layout Editor) version 4.16r2 Light Edition from CadSoft [171] has been used for producing the circuit schematics and for drawing the PCB layouts for all the circuits. The light edition of the software is capable of producing PCBs

with two signal layers, i.e. double sided PCBs, however, it has the limitation of a maximum PCB size of 100 x 80 mm. Due to the circuits being modular in nature, EAGLE provided adequate functionality to design all the PCBs that were needed throughout the course of the research.

A simplified circuit schematic is given in Figure 6.12. In depth discussions of the circuit then follow in §§6.5.1 – 6.5.4.

In brief, the circuit consists of the following sections:

1. Circuit inputs for selecting the mode (*read*, *write* or *erase*) and the PMD cell to be addressed.
2. Decoder for selecting the *read*, *write* or *erase* analogue switch.
3. Analogue switches for selecting *read*, *write* or *erase* voltages.
4. Analogue switch PMD row decoder.
5. Analogue switch PMD column decoder.
6. PMD.
7. Buffered inputs to operational amplifiers.
8. Reference input for operational amplifiers.
9. Operational amplifiers for determining the state of the PMD cells.
10. Comparators for providing a digital output of the memory state.

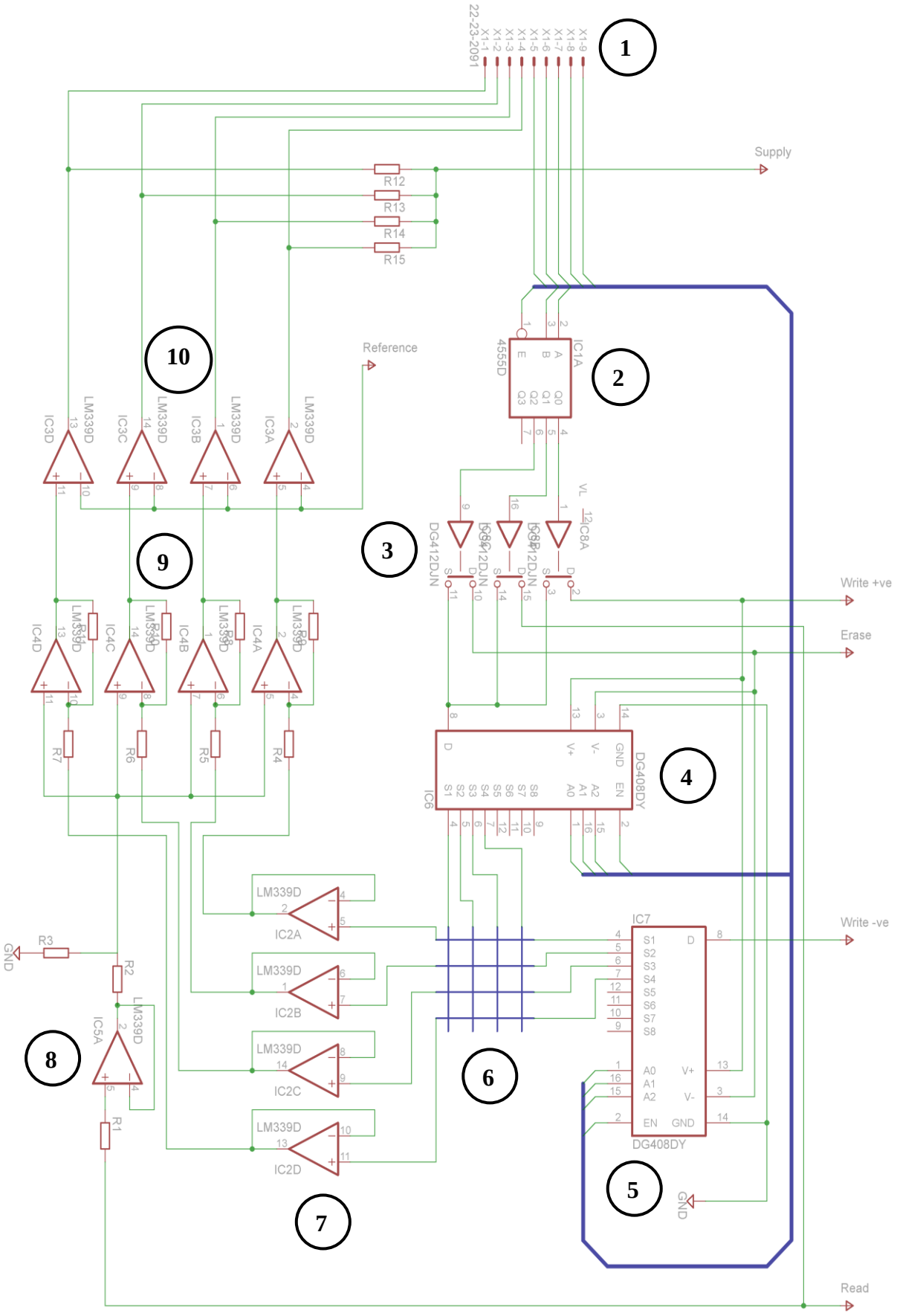


Figure 6.12 Simplified schematic of the PMD control and decoder circuitry.

6.5.1. Voltage Supplies

This board is capable of providing all the necessary voltages that the PMD needs for performing the *read*, *write* and *erase* functions, as well as supplying power for the accompanying logic circuitry. As many aspects of the PMDs electrical characteristics are variable between different device structures, specific *read*, *write* and *erase* voltages that are suitable for all PMDs are impossible to define. For these reasons, a large amount of flexibility has been designed into the voltage supply. LM317 and LM337 positive and negative adjustable voltage regulators respectively were selected as the basis of the circuit. Both regulators are capable of supplying voltages between 1.5 V and 37 V in their respective polarity and can supply up to 1.5 A of current, which far exceeds voltage and current requirements for any PMD used during this study.

When considering the voltage needs of the PMDs there are some subtle differences between how voltages are supplied when they are being controlled through circuitry, rather than directly from a probe station. These differences are particularly important when *write* pulses are applied to memory devices. Under probe station operation each memory cell is accessed individually. In most cases the row and column lines between cells are severed to ensure only the characteristics of the PMD under test are measured and to negate the array effects discussed in §6.1. In the remainder of cases when a voltage is applied to a row line, the unconnected column lines are at a floating voltage. Hence voltages applied to one memory cell have a minimal effect and in most cases no effect on surrounding memory cells, as illustrated in Figure 6.13(a). In this case the *write* voltage can be applied to the row line to switch the state of the memory. In contrast to this, Figure 6.13(b) illustrates how the interface circuits access the memory. In this situation all the column lines are connected to an analogue multiplexer, so any lines that aren't accessed are held at ground. Hence the full *write* voltage cannot be applied directly to the row, as this would bias all the cells on that row and switch the state of all the cells. As a result of this, the *write* voltage has to be applied in two parts, half to the row line and half to the column line, so the only cell biased with the full *write* voltage is at the location where the row and column lines cross.

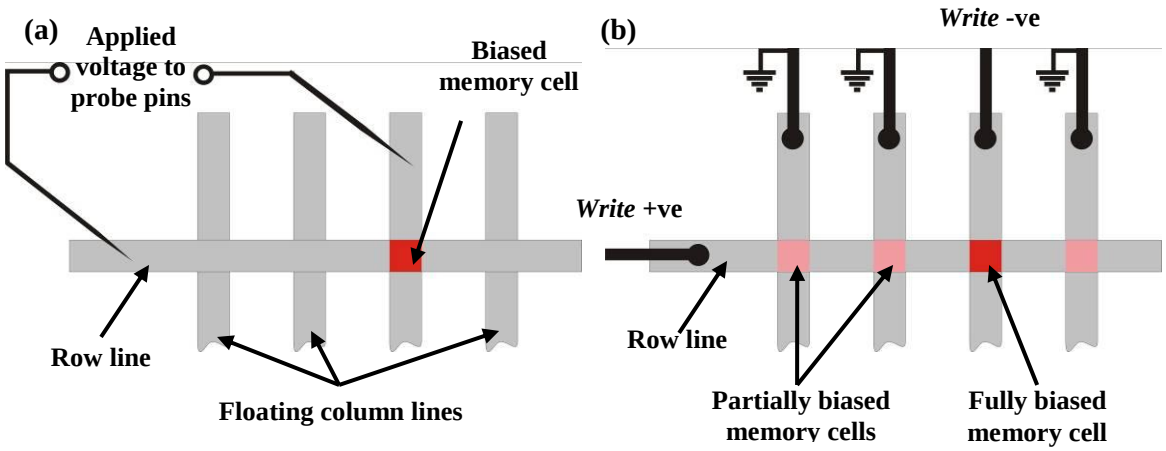


Figure 6.13 Voltage bias for (a) Probe station operation and (b) Circuit operation.

All the voltages that need to be supplied for PMD operation as well as supplying the voltages needed internally for the circuitry, are shown in Table 6.2. The maximum adjustment that is available on each voltage channel from the regulator is also given.

Table 6.2. Required Voltage Levels

Voltage Function	Voltage Name	Nominal Value (V)	Maximum Adjustment Available (V)
Logic chip supply	LOGIC	6.00	11.67
Analogue maximum	V+	10.00	11.67
Analogue minimum	V-	-10.00	-11.67
PMD *read*	READ	2.00	3.91
PMD *erase*	ERASE	-4.00	-9.58
PMD *write* positive	WRITE+	2.00	6.57
PMD *write* negative	WRITE-	-2.00	-9.58

Each voltage is supplied by a single regulator, with the exception of the two *write* voltages, which share supplies with the *read* and *erase* regulators. Whether the *read* and *erase* voltages, or the *write* voltage are being supplied is then determined digitally by setting a control input to a digital *1* when in *write* mode.

The full circuit schematic and PCB layout for the voltage supply can be found in Appendix J1.

6.5.2. Row Address Decoders

When polymer memory devices are interfaced via the circuit they are done so in a parallel nature, with one row of memory being accessed at a time during *read* cycles. During *write* or *erase* cycles the row of cells is addressed using the row address decoder, while the column is addressed by the PMD interface board, as discussed in §6.5.3. All PMDs fabricated during the course of the research either had four or eight rows of PMD cells, depending upon the device dimensions used. (Fewer cells could be made on each substrate when larger dimensions were used). However, the circuit designed is capable of addressing up to 128-rows of memory making it suitable for use in future projects where larger arrays of memories may be studied. With minor modifications it is also possible to address a further 128-rows, giving a total of 2048 memory cells (256-rows by 8-columns).

The ICs on this circuit are the main ones responsible for passing the *read*, *write* and *erase* voltages through to the rows of PMD cells. Due to the need for a range of voltages, simple digital address decoders cannot be used as the basis for the circuit. To overcome this, an array of analogue switches has been used, enabling any voltage to be passed through to the PMDs, with a particular switch being selected using a digital address decoder. A full circuit schematic and PCB layout of the address decoder circuit can be seen in Appendix J2.

6.5.3. Interface Board

The interface board has two separate functions. Firstly it provides the electrical contacts to both the row and column lines of the PMD, and secondly it provides the voltage to the column line of the memory during the *write* cycle, as discussed in §6.5.1.

One of the requirements for accessing the PMDs is the need to be able to access several memory cells at once, which is not easily achievable when a probe station is being used. The interface board is designed to easily provide electrical contacts to the PMD without the need for an array of probe pins. Several methods were investigated to accomplish this, with the first being the use of elastomeric conductors between the PMDs' contact pads and the PCB, allowing a reliable and simple contact to be made. (See Figure 6.14). This is the same technology conventionally used in connecting liquid crystal displays (LCDs) to PCBs, hence is a well known technology that has been used in many successful applications. The elastomeric conductors themselves consist of alternating bands of insulating and conducting rubber strips, which provide a vertical connection between contacts. To provide the best possible connection the pitch of the connector should be 4 – 5 times the pitch of the contact

pads, to allow multiple conduction paths and safeguard against misalignments between contacts. Due to the pitch restriction, contact pads down to approximately 200µm can be used with elastomeric connectors, making them suitable for all PMD generations that have been used throughout this research.

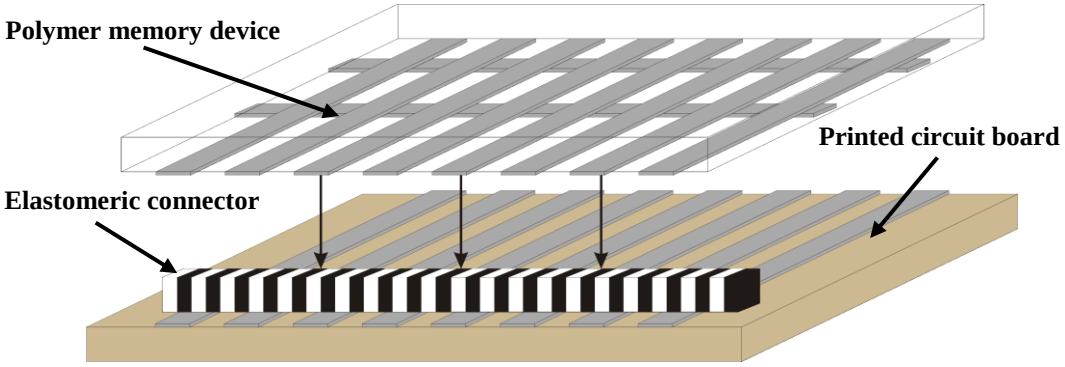


Figure 6.14 Elastomeric connector between PMD and PCB.

The second method is similar in principal to the elastomeric conductors, but replaces them with anisotropic conductive tape [172], providing both a mechanical adhesion between the PMD and PCB and an electrical connection between the two. This tape only conducts in the z-axis, so short circuiting of contacts is eliminated. The tape has the advantage of not requiring any further mechanical clamping of the PMD substrate to the PCB eliminating damage to the PMD. This particular specification of tape can be used with bond pad sizes down to ~3 mm^2, however, finer pitch tapes are available for use with bond pads <100 μm^2.

As memory cells with different dimensions have different contact pad sizes and layouts an interface PCB was designed for each layout used. In reality this meant that two boards were designed, one for memories based on 4-rows by 4-columns and the second for 8-row by 8-column devices. This means the interface board is the only circuit that is designed to work specifically with one generation of memory devices and as such can easily be replaced if it is necessary to connect to different configurations of PMDs. The circuit schematic and PCB layout for the two interface boards used can be seen in Appendix J3.

6.5.4. Output Circuitry

This circuit is responsible for decoding the state of each individual memory cell and outputting that data as a digital *1* or *0*. It also provides either a parallel data output that can subsequently be interfaced with a computer, or alternatively gives a visual indication of the

PMD output in the form of eight light emitting diodes (LEDs), representing the 8-bit wide row of memory that is currently being accessed.

To correctly decode the state of an individual memory cell a combination of analogue operational amplifiers and voltage comparators are used. The first stage of the decoding process utilises a differential amplifier, having one input as the voltage output of the memory cell being read and the other input being a reference voltage set by a variable resistor to be equivalent to the voltage output of a memory cell in its *off* state. The amplifier also has buffered inputs to provide the most stable configuration.

By using the amplifier in this configuration, when a memory cell is *off* the difference between the amplifier inputs is at a minimum, hence the amplified voltage is small. When the memory is in the *on* state the difference is at a maximum and hence the amplified voltage will be large in comparison with the *off* state.

This amplified voltage is then fed into a comparator circuit, which compares the output of the amplifiers to a reference voltage and provides a voltage at either ground, or the logic voltage level, depending upon whether the memory cell is *on* or *off*. This output can then either be used as an 8-bit wide parallel data stream for interfacing with a computer system, or alternatively can be directly viewed on the PCB via eight LEDs. The LED output under test conditions can be seen in Figure 6.15

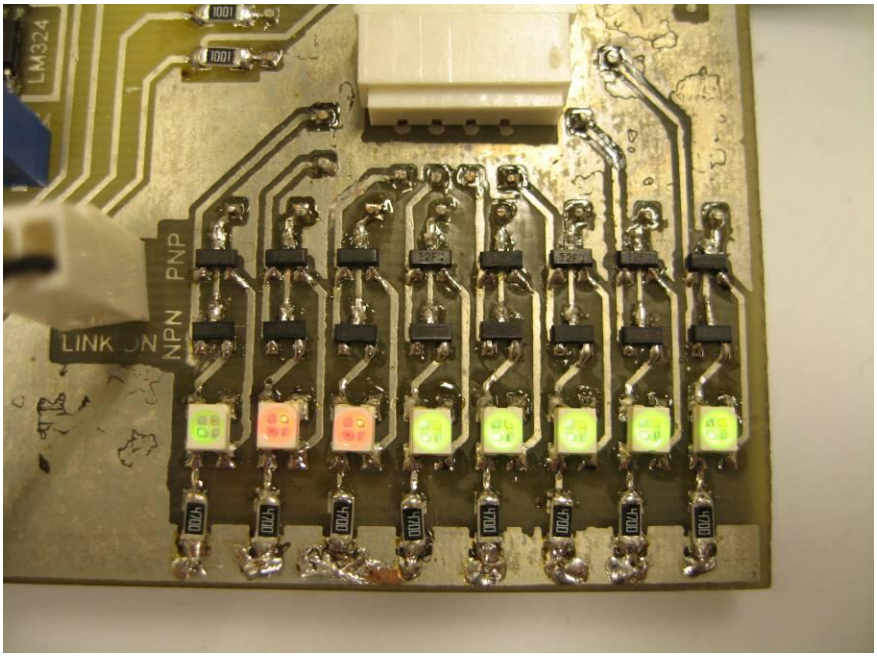


Figure 6.15 Memory decoder output showing 8-bits of test data.

The full circuit schematic for the output circuit and PCB layout can be found in Appendix J4.

6.6. Summary of Chapter 6

Gold nanoparticle based MIM memory devices have been fabricated and tested, with experimental results shown to differ greatly from those presented by Ouyang *et al*. [9]. In his, and many other devices presented in literature, abrupt switching occurs between the two different conductivity states of the memories. However, here O-shaped switching was found to occur with experimental data suggesting that a charge trapping mechanism is responsible for the hysteresis and memory effect.

Memory mechanisms for other characteristic *I-V* shapes have also been discussed, with S-shaped characteristics potentially related to electrode effects, either through oxide formation, or damage due to evaporated contacts. N-shaped characteristics were never observed during the project, so little experimental data can drawn upon, however, the theory of space charge fields limiting conduction and establishing NRD regions would appear to be the most plausible of the prevalent theories.

Control and interface circuitry has been demonstrated that is capable of interfacing to, and decoding PMDs in rows of parallel data, rather than single memory cells in serial as is accessed thus far with probe stations. Due to the lack of working PMDs, the circuitry has only been tested with simulated memory devices, replacing each cell with a known resistor value. These tests show that the circuitry is capable of decoding the memory state without error.

In addition, memory devices based on an MIS capacitor structure have been demonstrated. These devices are motivated from the principals of trapped charge in the insulator leading to shifts in the flatband capacitance. This characteristic was measured in §4.5 to investigate the properties of polystyrene, and also exploited in §5.2.6 to demonstrate the ability of gold nanoparticles to trap charge. These devices were shown to exhibit the basic characteristics needed for a memory device, with performance levels good enough for considering the future development of the memories. One of the main benefits of this structure is the known method of operation and predictable device parameters, meaning the structure can easily be tailored to suit specifications. The known method of operation also gives the benefit of having devices that operate reliably; a characteristic that is crucial for commercialisation of a device.

CHAPTER 7

Conclusions of the Research and Suggested Future Work

This chapter provides conclusions to the research and suggests possible directions that future research could take.

7.1. Conclusions

The research conducted in this thesis is primarily concerned with investigating the working mechanisms polymer memory devices, with a particular interest in PMDs containing nanoparticles. These memories have been categorised based on one of three distinguishing memory shapes in their *I-V* characteristics, namely; S, O and N-shaped characteristics.

S-shaped characteristics can further be split into two sub-categories; those with low *on* state currents of approximately a few hundred nanoamperes and those with larger *on* state currents (microamperes and above). For the former devices the proposed switching mechanism is as a result of electrode effects, with oxide formation likely at the metal-insulator interface. This interface will block the current flow resulting in the *off* state characteristics, while the *on* state characteristics are simply the normal conductivity level of the insulator layer. Devices characterised by high *on* state conductivities, especially with near ohmic conductivities are likely due to insulator breakdown and conduction through localised areas, or filaments. Break junction experiments have shown that microamperes currents and above cannot be supported by the PMD constituent materials and also that reproducible switching is possible from filament formation.

Experimental evidence supports the theory that nanoparticle charging is responsible for the hysteresis in O-shaped characteristics, however electrode effects could not be discounted completely. Further MIM devices manufactured with Type-II gold nanoparticles showed no evidence of hysteresis, highlighting the dependence of the memory effect on the constituent materials of the PMDs.

No devices investigated showed evidence of N-shaped characteristics, hence it is only possible to draw speculative conclusions here. Mechanisms based on SCLC do appear to be plausible and offer a qualitative explanation for the features of the *I-V* characteristics.

Polystyrene films in the nanometre thickness range have been thoroughly electrically characterised with trapped charge levels in the insulator found to be comparable to those in

silicon dioxide with fixed and insulator trapped charge densities and mobile trapped charge densities of 9.2×10^{11} cm^{-1} and 2.6×10^{12} cm^{-1} respectively. Mobile trapped charge was also found to be mobile at room temperature in polystyrene films. The maximum dielectric breakdown strength of the films was found to be 4.7 $MV \cdot cm^{-1}$, which is significantly higher than the manufacturers bulk value of 0.2 – 0.8 $MV \cdot cm^{-1}$, but is attributed to a change in breakdown mechanism when thin film devices are studied. Conduction mechanisms in polystyrene have also been investigated with the dominant conduction mechanism found to be Schottky emission.

Electrostatic force microscopy experiments have been conducted to further understand the nanoparticle charging in PMDs. EFM conducted on nanoparticle loaded polystyrene films was found to be an unreliable way for determining nanoparticle charging due to the influence of the polymer matrix. By eliminating the polystyrene layer and charging the nanoparticles via metal electrodes, unambiguous charging has been demonstrated. Charging effects can also be imaged at a high rate with this method, as the EFM tip is only used for imaging.

MIM and MIS gold nanoparticle PMDs have been demonstrated. The characteristics of both devices were found to require further improvement before being able to meet the minimum requirements for even a low cost, low specification memory. A problem with both types of PMDs was found to be the distribution in currents in the two memory states, which makes distinguishing the states difficult when considering large numbers of individual devices. In this respect MIS based PMDs offer the greatest potential for improving the distribution in characteristics, as they largely depend upon device geometry and variation in geometry.

Control and interface circuitry has been demonstrated that is capable of performing *read*, *write* and *erase* functions to multiple memory cells on a substrate in parallel.

7.2. Future Work

The next logical step in progression of the work continuing from this research would be to further investigate the hypothesis that electrode effects are responsible for the memory effect in many PMDs. The exact role that the top and bottom electrodes are each playing is still not well understood, with the role of evaporated top contacts still open to debate. The fabrication of structures containing deliberately introduced oxide layers on electrodes can further elucidate the switching mechanism. Alternative fabrication techniques should also be employed which would eliminate the role of the contacts to the working mechanisms

The scaling effects on memory characteristics need to be investigated to ensure the required *on/off* ratios can be achieved as the cell size is reduced. The variability between devices is also an issue. This may improve as dimensions are reduced and hence defects are reduced.

In order to produce PMDs that can be used in real world applications, ideally they should show rectification behaviour to ensure correct *read* cycles and prevent short circuits between memory cells.

The PMD control and interface circuits also need to be extended to allow computer control. This could be achieved by using a basic microcontroller with RS-232 data communication, allowing memory addresses and *read*, *write* or *erase* data to be sent by a computer, and memory state information to be returned by the PMD interface circuits.

References

1. H. Sirringhaus, T. Kawase, R. H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, and E. P. Woo. *High-resolution inkjet printing of all-polymer transistor circuits*. Science, 2000, **290**(5499), p.2123-2126.

2. F. Garnier, R. Hajlaoui, A. Yassar, and P. Srivastava. *All-Polymer Field-Effect Transistor Realized by Printing Techniques*. Science, 1994, **265**(5179), p.1684-1686.

3. J. C. Scott. *Is there an immortal memory?* Science, 2004, **304**(5667), p.62-63.

4. CBS Interactive Inc. *Moore's Law limit hit by 2014?* 2009 [cited 28/08/2009]; Available from: http://news.cnet.com/8301-13924_3-10265373-64.html.

5. ITRS. *International Technology Roadmap For Semiconductors 2007 Edition*. 2007 [cited 28/08/2009]; Available from: http://www.itrs.net/Links/2007ITRS/Home2007.htm.

6. D. Ma, M. Aguiar, J. A. Freire, and I. A. Hummelgen. *Organic reversible switching devices for memory applications*. Advanced Materials, 2000, **12**(14), p.1063-1066.

7. L. P. Ma, J. Liu, S. Pyo, Q. F. Xu, and Y. Yang. *Organic bistable devices*. Molecular Crystals and Liquid Crystals, 2002, **378**, p.185-192.

8. L. P. Ma, J. Liu, and Y. Yang. *Organic electrical bistable devices and rewritable memory cells*. Applied Physics Letters, 2002, **80**(16), p.2997-2999.

9. J. Y. Ouyang, C. W. Chu, C. R. Szmanda, L. P. Ma, and Y. Yang. *Programmable polymer thin film and non-volatile memory device*. Nature Materials, 2004, **3**(12), p.918-922.

10. J. Y. Ouyang, C. W. Chu, R. J. H. Tseng, A. Prakash, and Y. Yang. *Organic memory device fabricated through solution processing*. Proceedings of the IEEE, 2005, **93**(7), p.1287-1296.

11. Y. Yang, L. P. Ma, and J. H. Wu. *Organic thin-film memory*. Mrs Bulletin, 2004, **29**(11), p.833-837.

12. L. D. Bozano, B. W. Kean, M. Beinhoff, K. R. Carter, P. M. Rice, and J. C. Scott. *Organic materials and thin-film structures for cross-point memory cells based on trapping in metallic nanoparticles*. Advanced Functional Materials, 2005, **15**(12), p.1933-1939.

13. L. D. Bozano, B. W. Kean, V. R. Deline, J. R. Salem, and J. C. Scott. *Mechanism for bistability in organic memory elements*. Applied Physics Letters, 2004, **84**(4), p.607-609.

14. Y. Yang, J. Ouyang, L. P. Ma, R. J. H. Tseng, and C. W. Chu. *Electrical switching and bistability in organic/polymeric thin films and memory devices*. Advanced Functional Materials, 2006, **16**(8), p.1001-1014.

15. H. T. Lin, Z. W. Pei, J. R. Chen, G. W. Hwang, J. F. Fan, and Y. J. Chan. *A new nonvolatile bistable polymer-nanoparticle memory device*. IEEE Electron Device Letters, 2007, **28**(11), p.951-953.

16. J. Y. Ouyang, C. W. Chu, D. Sieves, and Y. Yang. *Electric-field-induced charge transfer between gold nanoparticle and capping 2-naphthalenethiol and organic memory cells*. Applied Physics Letters, 2005, **86**(12), p.123507.

17. M. Colle, M. Buchel, and D. M. de Leeuw. *Switching and filamentary conduction in non-volatile organic memories*. Organic Electronics, 2006, **7**(5), p.305-312.

18. Y. Noguchi, T. Nagase, T. Kubota, T. Kamikado, and S. Mashiko. *Fabrication of Au-molecule-Au junctions using electromigration method.* Thin Solid Films, 2006, **499**(1-2), p.90-94.

19. Answers Corporation. *Niels Bohr Biography*. 2009 [cited 25/08/2009]; Available from: http://www.answers.com/topic/niels-bohr.

20. J. Bardeen and W. H. Brattain. *The Transistor, A Semi-Conductor Triode*. Physical Review, 1948, **74**(2), p.230-231.

21. D. P. Mikkelson and B. Mikkelson. *GM Replies to Bill Gates*. 2005 [cited 26/08/2009]; Available from: http://www.snopes.com/humor/jokes/autos.asp.

22. Advanced Micro Devices. *AMD Demos 45nm Native Quad-Core Processors for Server, Desktop*. 2008 [cited 28/08/20009]; Available from: http://www.amd.com/us-en/Corporate/VirtualPressRoom/0,,51_104_543~124069,00.html.

23. Intel. *First 45nm Intel® Core™ Microarchitecture*. 2007 [cited 25/08/2009]; Available from: http://www.intel.com/technology/architecture-silicon/45nm-core2/index.htm?cid=emea:ggl|chips_uk_45nm|u4C558F|s.

24. Intel. *32nm Logic Technology*. 2009 [cited 28/08/2009]; Available from: http://www.intel.com/technology/architecture-silicon/32nm/index.htm?iid=tech_arch_45nm+rhc_32nm.

25. Intel. *Intel Architecture and Silicon Cadence*. 2006 [cited 28/09/2009]; Available from: http://isdlibrary.intel-dispatch.com/isd/201/cadence.pdf.

26. C. K. Chiang, C. R. Fincher, Y. W. Park, A. J. Heeger, H. Shirakawa, E. J. Louis, S. C. Gau, and A. G. Macdiarmid. *Electrical-Conductivity in Doped Polyacetylene*. Physical Review Letters, 1977, **39**(17), p.1098-1101.

27. C. W. Tang and S. A. Vanslyke. *Organic Electroluminescent Diodes*. Applied Physics Letters, 1987, **51**(12), p.913-915.

28. G. Yu, J. Gao, J. C. Hummelen, F. Wudl, and A. J. Heeger. *Polymer Photovoltaic Cells - Enhanced Efficiencies Via a Network of Internal Donor-Acceptor Heterojunctions*. Science, 1995, **270**(5243), p.1789-1791.

29. Sony. *XEL-1 (XEL1): Overview: Bravia TV: Sony*. 2007 [cited 15/08/2009]; Available from: http://www.sony.co.uk/product/tvp-oled-tv/xel-1.

30. Ebuyer. *Ebuyer - Hard Drives*. 2008 [cited 18/12/2008]; Available from: http://www.ebuyer.com/store/Components/cat/Hard-Drives.

31. Ebuyer. *Ebuyer - Flash Memory*. 2008 [cited 18/12/2008]; Available from: http://www.ebuyer.com/store/Components/cat/Flash-Memory.

32. Apple. *Macbook Air*. 2008 [cited 18/12/2008]; Available from: http://www.apple.com/macbookair/.

33. M. Julliere. *Tunneling between ferromagnetic films*. Physics Letters A, 1975, **54A**(3), p.225-6.

34. Everspin Technologies. *Everspin Technologies*. 2009 [cited 14/08/2009]; Available from: http://www.everspin.com/index.html.

35. Physikalisch Technische Bundesanstalt. *Method of ultra fast MRAM write operation*. 2004 [cited 14/08/2009]; Available from: http://www.ptb.de/s/c/JaRHA4aQ/patentDB_Dokumente/A45.pdf;jsessionid=19B271A1972C31D2891D02DCE607AFCC.

36. Onecall. *Everspin Technologies - MR2A16AYS35 - MRAM 4MB*. 2009 [cited 20/08/2009]; Available from: http://onecall.farnell.com/everspin-technologies/mr2a16ays35/mram-4mb-35ns-smd-tsop-ii-44/dp/1605454.

37. Ramtron. *Ramtron Product Detail: FM23MLD16*. 2009 [cited 24/8/2009]; Available from: http://www.ramtron.com/products/nonvolatile-memory/parallel-product.aspx?id=116.

38. Ramtron. *F-RAM Technology Brief*. 2007 [cited 24/08/2009]; Available from: http://www.ramtron.com/files/tech_papers/FerroelectricTechBrief.pdf.

39. Toshiba. *Toshiba Develops World's Highest Bandwidth, Highest Density Non-volatile RAM*. 2009 [cited; Available from: http://www.toshiba.com/taec/news/press_releases/2009/memy_09_554.jsp.

40. EFY Enterprises Pvt Ltd. *Ramtron Launches 8Mb F-RAM Memory*. 2009 [cited 24/08/2009]; Available from: http://www.efytimes.com/efytimes/35733/news.htm.

41. W. Y. Cho, B. H. Cho, B .G. Choi, H. R. Oh, S. Kang, K .S. Kim, K. H. Kim, D. E. Kim, C. K. Kwak, H. G. Byun, Y. Hwang, S. Ahn, G. H. Koh, G. Jeong, H. Jeong, and K. Kim. *A 0.18-m 3.0-V 64-Mb nonvolatile phase-transition random access memory (PRAM)*. IEEE Journal of Solid-State Circuits, 2005, **40**(1), p.293-300.

42. ITRS. *International Technology Roadmap For Semiconductors 2007 Edition - Emerging Research Devices*. 2007 [cited 10/07/2009]; Available from: http://www.itrs.net/Links/2007ITRS/2007_Chapters/2007_ERD.pdf.

43. Numonyx. *Intel, STMicroelectronics Deliver Industry's First Phase Change Memory Prototypes*. 2008 [cited 24/07/2009]; Available from: http://www.numonyx.com/en-US/About/PressRoom/Releases/Pages/IntelSTDeliverFirstPCMPrototypes.aspx.

44. Samsung. *Samsung Electronics and Numonyx Join Forces on Phase Change Memory*. 2009 [cited 24/07/2009]; Available from: http://www.samsung.com/us/business/semiconductor/newsView.do?news_id=1023.

45. J. W. Kang, J. H. Lee, H. J. Lee, and H .J. Hwang. *A study on carbon nanotube bridge as a electromechanical memory device*. Physica E, 2005, **27**(3), p.332-40.

46. Nantero Inc. *Nantero*. 2009 [cited 19/07/2009]; Available from: http://www.nantero.com.

47. IBM. *Magnetic Racetrack Memory Project*. 2009 [cited 24/07/2009]; Available from: http://www.almaden.ibm.com/spinaps/research/sd/?racetrack.

48. S. S. P. Parkin, M. Hayashi, and L. Thomas. *Magnetic Domain-Wall Racetrack Memory*. Science, 2008, **320**(5873), p.190-194.

49. M. Hayashi, L. Thomas, R. Moriya, C. Rettner, and S. S. P. Parkin. *Current-Controlled Magnetic Domain-Wall Nanowire Shift Register*. Science, 2008, **320**(5873), p.209-211.

50. G. Meier, M. Bolte, R. Eiselt, B. Kruger, D. H. Kim, and P. Fischer. *Direct Imaging of Stochastic Domain-Wall Motion Driven by Nanosecond Current Pulses*. Physical Review Letters, 2007, **98**(18), p.187202.

51. Institute of Engineering and Technology. *Resistance is not futile*. 2008 [cited 23/08/2009]; Available from: http://kn.theiet.org/magazine/issues/0816/resistance-0816.cfm.

52. 4DS Inc. *4DS Non-Volatile Memory to Disrupt $60B Market*. 2009 [cited 20/08/2009]; Available from: http://www.4-d-s.com/news_release_090210.html.

53. T. W. Hickmott. *Low-Frequency Negative Resistance in Thin Anodic Oxide Films*. Journal of Applied Physics, 1962, **33**(9), p.2669-2682.

54. T. W. Hickmott. *Electron Emission, Electroluminescence, and Voltage-Controlled Negative Resistance in Al-AlO_2-Au Diodes*. Journal of Applied Physics, 1965, **36**(6), p.1885-1896.

55. C. Barriac. *Study of the electrical properties of Al-Al_2O_3-metal structures*. Physica Status Solidi A - Applied Research, 1969, **34**(2), p.621-633.

56. J. G. Simmons and R. R. Verderber. *New Conduction and Reversible Memory Phenomena in Thin Insulating Films*. Proceedings of the Royal Society of London. Series A., 1967, **301**, p.77-102.

57. R. R Sutherland. *Theory for Negative Resistance and Memory Effects in Thin Insulating Films and Its Application to Au-ZnS-Au Devices*. Journal of Physics D - Applied Physics, 1971, **4**(3), p.468-479.

58. A. A. Ansari and A. Qadeer. *Memory Switching in Thermally Grown Titanium-Oxide Films*. Journal of Physics D - Applied Physics, 1985, **18**(5), p.911-917.

59. C. A. Hogarth and M. Zor. *Some Observations of Voltage-Induced Conductance Changes in Thin-Films of Evaporated Polyethylene*. Thin Solid Films, 1975, **27**(1), p.L5-L7.

60. C. A. Hogarth and T. Iqbal. *Electroforming of Thin-Films of Polypropylene*. International Journal of Electronics, 1979, **47**(4), p.349-353.

61. G. Dearnaley. *A Model for Filament Growth and Switching in Amorphous Oxide Films*. Journal of Non-Crystalline Solids, 1970, **4**, p.593-612.

62. H. Biederman, H. Lehmberg, and H. Pagnia. *On the Source of Current-Carrying Filament Material in Mim-Diodes*. Vacuum, 1989, **39**(1), p.27-28.

63. R. Blessing, K. H. Gurtler, and H. Pagnia. *Switching of Point-Contact Diodes Consisting of Discontinuous Gold-Films*. Physics Letters A, 1981, **84**(6), p.341-344.

64. R. E. Thurstans and D. P. Oxley. *The electroformed metal-insulator-metal structure: a comprehensive model*. Journal of Physics D - Applied Physics, 2002, **35**(8), p.802-809.

65. C. Cen, S. Thiel, G. Hammerl, C. W. Schneider, K. E. Andersen, C. S. Hellberg, J. Mannhart, and J. Levy. *Nanoscale control of an interfacial metal-insulator transition at room temperature*. Nature Materials, 2008, **7**(4), p.298-302.

66. H. Pagnia. *Metal-Insulator-Metal Devices with Carbonaceous Current Paths*. International Journal of Electronics, 1990, **69**(1), p.33-42.

67. A. K. Ray and C. A. Hogarth. *A Critical-Review of the Observed Electrical-Properties of MIM Devices Showing VCNR*. International Journal of Electronics, 1984, **57**(1), p.1-77.

68. A. K. Ray and C. A. Hogarth. *Recent Advances in the Polyfilamentary Model for Electronic Conduction in Electroformed Insulating Films*. International Journal of Electronics, 1990, **69**(1), p.97-107.

69. H. Pagnia, K. Schlemper, and N. Sotnik. *Studies of Electroformed Gold Island Film Diodes under Bias in a TEM*. Materials Letters, 1987, **5**(7-8), p.260-262.

70. H. Pagnia, N. Sotnik, and W. Wirth. *Scanning Tunneling Microscopic Investigations of Electroformed Planar Metal-Insulator-Metal Diodes*. International Journal of Electronics, 1990, **69**(1), p.25-32.

71. S. Brauer, H. Pagnia, and N. Sotnik. *The Filamentary Model of Electroformed MIM Devices - Still up-to-Date*. International Journal of Electronics, 1994, **76**(5), p.707-711.

72. H. Pagnia. *Memory States In Electroformed MIM Diodes*. International Journal Of Electronics, 1994, **76**(5), p.695-705.

73. S. Moller, C. Perlov, W. Jackson, C. Taussig, and S. R. Forrest. *A polymer/semiconductor write-once read-many-times memory*. Nature, 2003, **426**(6963), p.166-169.

74. J. Chen, M. A. Reed, A. M. Rawlett, and J. M. Tour. *Large on-off ratios and negative differential resistance in a molecular electronic device*. Science, 1999, **286**(5444), p.1550-1552.

75. M. A. Reed, J. Chen, A. M. Rawlett, D. W. Price, and J. M. Tour. *Molecular random access memory cell*. Applied Physics Letters, 2001, **78**(23), p.3735-3737.

76. Y. Chen, G. Y. Jung, D. A. A. Ohlberg, X. M. Li, D. R. Stewart, J. O. Jeppesen, K. A. Nielsen, J. F. Stoddart, and R. S. Williams. *Nanoscale molecular-switch crossbar circuits*. Nanotechnology, 2003, **14**(4), p.462-468.

77. Y. Chen, D. A. A. Ohlberg, X. M. Li, D. R. Stewart, R. S. Williams, J. O. Jeppesen, K. A. Nielsen, J. F. Stoddart, D. L. Olynick, and E. Anderson. *Nanoscale molecular-switch devices fabricated by imprint lithography*. Applied Physics Letters, 2003, **82**(10), p.1610-1612.

78. A. Bandyopadhyay and A. J. Pal. *Key to design functional organic molecules for binary operation with large conductance switching*. Chemical Physics Letters, 2003, **371**(1-2), p.86-90.

79. A. Bandyopadhyay and A. J. Pal. *Large conductance switching and memory effects in organic molecules for data-storage applications*. Applied Physics Letters, 2003, **82**(8), p.1215-1217.

80. S. K. Majee, A. Bandyopadhyay, and A. J. Pal. *Electrical bistability in molecular films: transition from memory to threshold switching*. Chemical Physics Letters, 2004, **399**(1-3), p.284-288.

81. F. L. E. Jakobsson, X. Crispin, M. Colle, M. Buchel, D. M. de Leeuw, and M. Berggren. *On the switching mechanism in Rose Bengal-based memory devices*. Organic Electronics, 2007, **8**(5), p.559-565.

82. L. P. Ma, J. Liu, S. M. Pyo, and Y. Yang. *Organic bistable light-emitting devices*. Applied Physics Letters, 2002, **80**(3), p.362-364.

83. L. P. Ma, S. Pyo, J. Ouyang, Q. F. Xu, and Y. Yang. *Nonvolatile electrical bistability of organic/metal-nanocluster/organic system*. Applied Physics Letters, 2003, **82**(9), p.1419-1421.

84. J. He, L. P. Ma, J. H. Wu, and Y. Yang. *Three-terminal organic memory devices*. Journal of Applied Physics, 2005, **97**(6), p.064507.

85. S. Pyo, L. P. Ma, J. He, Q. F. Xu, Y. Yang, and Y. L. Gao. *Experimental study on thickness-related electrical characteristics in organic/metal-nanocluster/organic systems*. Journal of Applied Physics, 2005, **98**(5), p.054303.

86. D. Tondelier, K. Lmimouni, D. Vuillaume, C. Fery, and G. Haas. *Metal/organic/metal bistable memory devices*. Applied Physics Letters, 2004, **85**(23), p.5763-5765.

87. S. Paul, C. Pearson, A. Molloy, M. A. Cousins, M. Green, S. Kolliopoulou, P. Dimitrakis, P. Normand, D. Tsoukalas, and M. C. Petty. *Langmuir-Blodgett film deposition of metallic nanoparticles and their application to electronic memory structures*. Nano Letters, 2003, **3**(4), p.533-536.

88. W. L. Leong, P. S. Lee, S. G. Mhaisalkar, T. P. Chen, and A. Dodabalapur. *Charging phenomena in pentacene-gold nanoparticle memory device*. Applied Physics Letters, 2007, **90**(4), p.042906.

89. E. Castella and C. K. Prout. *Molecular Complexes .10. Crystal and Molecular Structure of 1-1 Complex of 8-Hydroxyquinoline and 1,3,5-Trinitrobenzene*. Journal of the Chemical Society A - Inorganic Physical Theoretical, 1971, (3), p.550-553.

90. D. M. Adams, L. Brus, C. E. D. Chidsey, S. Creager, C. Creutz, C. R. Kagan, P. V. Kamat, M. Lieberman, S. Lindsay, R. A. Marcus, R. M. Metzger, M. E. Michel-Beyerle, J. R. Miller, M. D. Newton, D. R. Rolison, O. Sankey, K. S. Schanze, J. Yardley, and X. Y. Zhu. *Charge transfer on the nanoscale: Current status*. Journal of Physical Chemistry B, 2003, **107**(28), p.6668-6697.

91. B. I. Ipe, K. G. Thomas, S. Barazzouk, S. Hotchandani, and P. V. Kamat. *Photoinduced charge separation in a fluorophore-gold nanoassembly*. Journal of Physical Chemistry B, 2002, **106**(1), p.18-21.

92. D. Prime and S. Paul. *Making Plastic Remember: Electrically Rewritable Polymer Memory Devices*. Materials Research Society Symposium Proceedings, 2007, **997**, p.21-25.

93. D. Prime and S. Paul. *Gold Nanoparticle Based Electrically Rewritable Polymer Memory Devices*. Advances In Science and Technology, 2008, **54**, p.480-485.

94. A. Prakash, J. Ouyang, J. L. Lin, and Y. Yang. *Polymer memory device based on conjugated polymer and gold nanoparticles*. Journal of Applied Physics, 2006, **100**(5), p.054309.

95. Y. Song, Q. D. Ling, S. L. Lim, E. Y. H. Teo, Y. P. Tan, L. Li, E. T. Kang, D. S. H. Chan, and C. X. Zhu. *Electrically bistable thin-film device based on PVK and GNPs polymer material*. IEEE Electron Device Letters, 2007, **28**(2), p.107-110.

96. V. S. Reddy, S. Karak, S. K. Ray, and A. Dhar. *Carrier transport mechanism in aluminum nanoparticle embedded AlQ3 structures for organic bistable memory devices*. Organic Electronics, 2009, **10**(1), p.138-44.

97. V. S. Reddy, S. Karak, and A. Dhar. *Multilevel conductance switching in organic memory devices based on AlQ3 and Al/Al2O3 core-shell nanoparticles*. Applied Physics Letters, 2009, **94**(17), p.173304.

98. R. J. Tseng, C. L. Tsai, L. P. Ma, and J. Y. Ouyang. *Digital memory device based on tobacco mosaic virus conjugated with nanoparticles*. Nature Nanotechnology, 2006, **1**(1), p.72-77.

99. A. Kanwal, S. Paul, and M. Chhowalla. *Organic memory devices using C/sub 60/ and insulating polymer*. Materials Research Society Symposium Proceedings, 2005, **Vol.830**, p.p 349-53.

100. H. S. Majumdar, J. K. Baral, R. Osterbacka, O. Ikkala, and H. Stubb. *Fullerene-based bistable devices and associated negative differential resistance effect*. Organic Electronics, 2005, **6**(4), p.188-192.

101. S. Paul, A. Kanwal, and M. Chhowalla. *Memory effect in thin films of insulating polymer and C-60 nanocomposites*. Nanotechnology, 2006, **17**(1), p.145-151.

102. L. P. Ma, Q. F. Xu, and Y. Yang. *Organic nonvolatile memory by controlling the dynamic copper-ion concentration within organic layer*. Applied Physics Letters, 2004, **84**(24), p.4908-4910.

103. Q. D. Ling, Y. Song, S. J. Ding, C. X. Zhu, D. S. H. Chan, D. L. Kwong, E. T. Kang, and K. G. Neoh. *Non-volatile polymer memory device based on a novel copolymer of*

N-vinylcarbazole and Eu-complexed vinylbenzoate. Advanced Materials, 2005, **17**(4), p.455-459.

104. S. K. Majee, H. S. Majumdar, A. Bolognesi, and A. J. Pal. *Electrical bistability and memory applications of poly(p-phenylenevinylene) films*. Synthetic Metals, 2006, **156**(11-13), p.828-832.

105. B. Pradhan, S. K. Batabyal, and A. J. Pal. *Electrical bistability and memory phenomenon in carbon nanotube-conjugated polymer matrixes*. Journal of Physical Chemistry B, 2006, **110**(16), p.8274-8277.

106. R. Bahri. *Solution-Grown Thin Polystyrene Films 1: DC Electrical Conduction*. Journal of Physics D - Applied Physics, 1982, **15**(4), p.677-687.

107. K. Efimenko, V. Rybka, V. Svorcik, and V. Hnatowicz. *Mechanism of conductivity in metal-polymer-metal structures*. Applied Physics A - Materials Science & Processing, 1999, **68**(4), p.479-482.

108. R. Bahri. *Solution-Grown Thin Polystyrene Films 2. Dielectric Properties*. Journal of Physics D - Applied Physics, 1982, **15**(4), p.689-696.

109. K. Efimenko, V. Rybka, V. Svorcik, and V. Hnatowicz. *Electrical properties of Au-polystyrene-Au submicron structures*. Applied Physics A - Materials Science & Processing, 1998, **67**(5), p.503-505.

110. Oxford University Press, *Oxford English Dictionary - Insulator*. 1989, Oxford University Press.

111. S. M. Sze, *Physics of Semiconductor Devices.* Second Edition ed. 1981: John Wiley and Sons.

112. M. Campos, E. M. Cavalcante, and J. Kalinowski. *Poole-Frenkel effect in amorphous poly(p-phenylene sulfide)*. Journal of Polymer Science Part B - Polymer Physics, 1996, **34**(4), p.623-629.

113. B. Thomas, M. G. K. Pillai, and S. Jayalekshmi. *On the Mechanism of Electrical-Conduction in Plasma-Polymerized Thiophene Thin-Films*. Journal of Physics D - Applied Physics, 1988, **21**(3), p.503-508.

114. G. Binnig, H. Rohrer, Gerber Ch, and E. Weibel. *Tunneling through a controllable vacuum gap*. 1982, **40**(2), p.178-180.

115. G. Binnig and H. Rohrer. *The Scanning Tunneling Microscope*. Scientific American, 1985, **253**(2), p.50-56.

116. G. Binnig, C. F. Quate, and Ch Gerber. *Atomic Force Microscope*. Physical Review Letters, 1986, **56**(9), p.930-933.

117. W. Bolton, *Newnes Engineering Materials*. Third Edition ed. 2000, Oxford: Newnes.

118. J. Brandrup and E. H Immergut, *Common Solvents and Non-Solvents of Polystyrene*, in *Polymer Handbook, Second Edition*. 1975.

119. International Labour Organization. *Polystyrene Data Sheet*. 2003 [cited 5/01/2009]; Available from: http://www.ilo.org/public/english/protection/safework/cis/products/icsc/dtasht/_icsc10/icsc1043.htm.

120. Y. P. Koh, G. B. McKenna, and S. L. Simon. *Calorimetric glass transition temperature and absolute heat capacity of polystyrene ultrathin films*. Journal of Polymer Science Part B - Polymer Physics, 2006, **44**(24), p.3518-3527.

121. L. Singh, P. J. Ludovice, and C. L. Henderson. *Influence of molecular weight and film thickness on the glass transition temperature and coefficient of thermal expansion of supported ultrathin polymer films*. Thin Solid Films, 2004, **449**(1-2), p.231-241.

122. Matweb. *Overview of materials for Polystyrene*. 2008 [cited 04/12/2008]; Available from: http://www.matweb.com/SpecificMaterial.asp?bassnum=O4800.

123. H. K. Kim and F. G. Shi. *Thickness dependent dielectric strength of a low-permittivity dielectric film*. IEEE Transactions on Dielectrics and Electrical Insulation, 2001, **8**(2), p.248-252.

124. C. Laurent, E. Kay, and N. Souag. *Dielectric-Breakdown of Polymer-Films Containing Metal-Clusters*. Journal of Applied Physics, 1988, **64**(1), p.336-343.

125. J.K. Barbalace. *Periodic Table of the Elements*. 2009 [cited 16/07/2009]; Available from: http://environmentalchemistry.com/yogi/periodic/.

126. Shin-Etsu. *Shin-Etsu Product Information*. 2008 [cited 15/01/2007]; Available from: http://www.shinetsu.co.jp/e/product/semicon.shtml.

127. E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. 1982, New York: John Wiley and Sons.

128. D. K. Schroder, *Semiconductor Material and Device Characterization.* Third Edition ed. 1998, New Jersey: John Wiley and Sons.

129. M. Yun, R. Ravindran, M. Hossain, S. Gangopadhyay, U. Scherf, T. Bunnagel, F. Galbrecht, M. Arif, and S. Guha. *Capacitance-voltage characterization of polyfluorene-based metal-insulator-semiconductor diodes*. Applied Physics Letters, 2006, **89**(1), p.013506.

130. S. Grecu, M. Bronner, A. Opitz, and W. Brutting. *Characterization of polymeric metal-insulator-semiconductor diodes*. Synthetic Metals, 2004, **146**(3), p.359-363.

131. V. Jacobsen, T. Zhu, W. Knoll, and M. Kreiter. *Current-Voltage Characterisation of Monolayer-Supported Au-Nanoclusters by Scanning Tunnelling Microscopy under Ambient Conditions*. 2005, **2005**(18), p.3683-3690.

132. G. A. O'Brien, A. J. Quinn, M. Biancardo, J. A. Preece, C. A. Bignozzi, and G. Redmond. *Making electrical nanocontacts to nanocrystal assemblies: mapping of room-temperature Coulomb-blockade thresholds in arrays of 28-kDa gold nanocrystals*. Small, 2006, **2**(2), p.261-6.

133. G. H. Yang, L. Tan, Y. Y. Yang, S. W. Chen, and G. Y. Liu. *Single electron tunneling and manipulation of nanoparticles on surfaces at room temperature*. Surface Science, 2005, **589**(1-3), p.129-138.

134. H. Graf, J. Vancea, and H. Hoffmann. *Single-electron tunneling at room temperature in cobalt nanoparticles*. Applied Physics Letters, 2002, **80**(7), p.1264-1266.

135. K. B. Blodgett. *Films Built by Depositing Successive Monomolecular Layers on a Solid Surface*. Journal of the American Chemical Society, 1935, **57**(6), p.1007-1022.

136. K. B. Blodgett and I. Langmuir. *Built-Up Films of Barium Stearate and Their Optical Properties*. Physical Review, 1937, **51**(11), p.964-982.

137. M. C. Petty, *Langmuir-Blodgett Films - An Introduction.* 1996, Cambridge: Cambridge University Press.

138. L. Di and L. Jinghong. *Preparation, characterization and quantized capacitance of 3-mercapto-1,2-propanediol monolayer protected gold nanoparticles*. Chemical Physics Letters, 2003, **372**(5-6), p.668-73.

139. M. B. Cortie, M. H. Zareie, S. R. Ekanayake, and M. J. Ford. *Conduction, storage, and leakage in particle-on-SAM nanocapacitors*. IEEE Transactions on Nanotechnology, 2005, **4**(4), p.406-14.

140. H. Zhang, Y. Yasutake, Y. Shichibu, T. Teranishi, and Y. Majima. *Tunneling resistance of double-barrier tunneling structures with an alkanethiol-protected Au nanoparticle*. Physical Review B, 2005, **72**(20), p.205441-1.

141. P. W. Josephs-Franks. *Variable temperature UHV STM facility.* [cited 2009 17/02/2009]; Available from: http://www.npl.co.uk/upload/pdf/CryoSTM_Spec.pdf.

142. NPL. *National Physical Laboratory, UK*. 2009 [cited 17/01/2009]; Available from: http://www.npl.co.uk/.

143. D. Prime, S. Paul, C. Pearson, M. Green, and M. C. Petty. *Nanoscale patterning of gold nanoparticles using an atomic force microscope*. Materials Science & Engineering C - Biomimetic and Supramolecular Systems, 2005, **25**(1), p.33-8.

144. D. M. Schaadt, E. T. Yu, S. Sankar, and A. E. Berkowitz. *Charge storage in Co nanoclusters embedded in SiO_2 by scanning force microscopy*. Applied Physics Letters, 1999, **74**(3), p.472-4.

145. J. Y. Yang, J. H. Kim, J. S. Lee, S. K. Min, H. J. Kim, K. L. Wang, and J. P. Hong. *Electrostatic force microscopy measurements of charge trapping behavior of Au nanoparticles embedded in metal-insulator-semiconductor structure*. Ultramicroscopy, 2008, **108**(10), p.1215-1219.

146. E. A. Boer, L. D. Bell, M. L. Brongersma, H. A. Atwater, M. L. Ostraat, and R. C. Flagan. *Charging of single Si nanocrystals by atomic force microscopy*. Applied Physics Letters, 2001, **78**(20), p.3133-5.

147. C. Y. Ng, T. P. Chen, H. W. Lau, Y. Liu, M. S. Tse, O. K. Tan, and V. S. W. Lim. *Visualizing charge transport in silicon nanocrystals embedded in SiO[sub 2] films with electrostatic force microscopy*. Applied Physics Letters, 2004, **85**(14), p.2941-2943.

148. Park Systems. *EFM probes - NSC36, Cr-Au*. 2009 [cited 12/01/2009]; Available from: http://www.psiastore.com/product.sc;jsessionid=FB69DF1A0DE0016A119E37301876E72F.qscstrfrnt01?categoryId=7&productId=112.

149. M. A. Rampi, O. J. A. Schueller, and G. M. Whitesides. *Alkanethiol self-assembled monolayers as the dielectric of capacitors with nanoscale thickness*. Applied Physics Letters, 1998, **72**(14), p.1781-3.

150. Corning. *Thermal Properties of Corning Glasses*. 2008 [cited 06/02/2009]; Available from: http://catalog2.corning.com/Lifesciences/media/pdf/Thermal_Properties_of_Corning_Glasses.pdf.

151. S. M. Sze, *Semiconductor Devices Physics and Technology*. Second Edition ed. 2002, New Jersey: John Wiley and Sons.

152. B. J. Kailath, A. DasGupta, and N. DasGupta. *Electrical and reliability characteristics of MOS devices with ultrathin SiO_2 grown in nitric acid solutions*. IEEE Transactions on Device and Materials Reliability, 2007, **7**(4), p.602-10.

153. H. Kobayashi, Asuha, O. Maida, M. Takahashi, and H. Iwasa. *Nitric acid oxidation of Si to form ultrathin silicon dioxide layers with a low leakage current density*. Journal of Applied Physics, 2003, **94**(11), p.7328-35.

154. V. Svorcik, V. Rybka, K. Efimenko, and V. Hnatowicz. *Deposition of polystyrene films by vacuum evaporation*. Journal of Materials Science Letters, 1997, **16**(19), p.1564-6.

155. Sigma-Aldrich. *Dodecanethiol functionalized gold nanoparticles Batch 04918MH Certificate of Analysis*. 2007 [cited 2009 02/08/2009]; Available from: http://www.sigmaaldrich.com/catalog/CertOfAnalysisPage.do?symbol=660434&LotNo=04918MH&brandTest=ALDRICH.

156. Wei Lin Leong, Pooi See Lee, Anup Lohani, Yeng Ming Lam, Tupei Chen, Sam Zhang, Ananth Dodabalapur, and Subodh G. Mhaisalkar. *Non-Volatile Organic Memory Applications Enabled by In Situ Synthesis of Gold Nanoparticles in a Self-Assembled Block Copolymer*. Advanced Materials, 2008, **20**, p.2325–2331.

157. W.H. Preece. *On the Heating Effects of Electric Currents*. Proceedings of the Royal Society of London, 1883, (36), p.464-471.

158. D. G. Fink and H. W. Beaty, *Standard Handbook for Electrical Engineers*. Vol. 14th. 1999: McGraw-Hill.

159. S. H. Kim, K. S. Yook, J. Jang, and J. Y. Lee. *Correlation of memory characteristics of polymer bistable memory devices with metal deposition process*. Synthetic Metals, 2008, **158**(21-24), p.861-864.

160. P. Dimitrakis, P. Normand, D. Tsoukalas, C. Pearson, J. H. Ahn, M. F. Mabrook, D. A. Zeze, M. C. Petty, K. T. Kamtekar, Wang Changsheng, M. R. Bryce, and M. Green. *Electrical behavior of memory devices based on fluorene-containing organic thin films*. Journal of Applied Physics, 2008, **104**(4), p.044510.

161. M. Terai, K. Fujita, and T. Tsutsui. *Highly Reproducible Electric Bistability in an Organic Single Layer Device with Ag Top Electrode*. Materials Research Society Symposium Proceedings, 2007, **965**, p.31-36.

162. S. Baek, D. Lee, J. Kim, S. H. Hong, O. Kim, and M. Ree. *Novel digital nonvolatile memory devices based on semiconducting polymer thin films*. Advanced Functional Materials, 2007, **17**(15), p.2637-2644.

163. H. T. Lin, Z. Pei, and Y. J. Chan. *Carrier transport mechanism in a nanoparticle-incorporated organic bistable memory device*. IEEE Electron Device Letters, 2007, **28**(7), p.569-71.

164. Q. D. Ling, D. J. Liaw, E. Y. H. Teo, C. X. Zhu, D. S. H. Chan, E. T. Kang, and K. G. Neoh. *Polymer memories: Bistable electrical switching and device performance*. Polymer, 2007, **48**(18), p.5182-5201.

165. EMTERC. *Emerging Technologies Research Centre*. 2008 [cited 23/02/2009]; Available from: http://www.cse.dmu.ac.uk/~dwatts/emterc//emterc_home_page_v2.htm.

166. J. C. Scott and L. D. Bozano. *Nonvolatile memory elements based on organic materials*. Advanced Materials, 2007, **19**(11), p.1452-1463.

167. J. H. Jung and T. W. Kim. *The effects of trap density on current bistability and negative differential resistance in organic bistable devices*. Solid State Communications, 2009, **149**(25-26), p.1025-1028.

168. S. Kolliopoulou, P. Dimitrakis, P. Normand, Zhang Hao-Li, N. Cant, S. D. Evans, S. Paul, C. Pearson, A. Molloy, M. C. Petty, and D. Tsoukalas. *Hybrid silicon-organic nanoparticle memory device*. Journal of Applied Physics, 2003, **94**(8), p.5234-9.

169. S. Kolliopoulou, P. Dimitrakis, P. Normand, H. L. Zhang, N. Cant, S. D. Evans, S. Paul, C. Pearson, A. Molloy, M. C. Petty, and D. Tsoukalas. *Integration of organic insulator and self-assembled gold nanoparticles on Si MOSFET for novel non-volatile memory cells*. Microelectronic Engineering, 2004, **73-74**, p.725-729.

170. M. F. Mabrook, C. Pearson, D. Kolb, D. A. Zeze, and M. C. Petty. *Memory effects in hybrid silicon-metallic nanoparticle-organic thin film structures*. Organic Electronics, 2008, **9**(5), p.816-20.

171. CadSoft, *EAGLE 4.16r2*. 2009. Available from: http://www.cadsoftusa.com

172. 3M. *3M Electrically Conductive Tape 9703*. 2009 [cited 12/07/09]; Available from: http://solutions.3m.com/wps/portal/3M/en_US/3MElectrical/Home/ProductsServices/Products/?PC_7_RJH9U5230GE3E02LECIE20OES1_nid=KKW6TLG05Mbe2R3TDRZMR3gl.

173. P. J. Mohr, B. N. Taylor, and D Newell, B. *CODATA recommended values of the fundamental physical constants: 2006*. Reviews of Modern Physics, 2008, **80**(2), p.633-98.

174. A. B. Sproul and M. A. Green. *Improved value for the silicon intrinsic carrier concentration from 275 to 375 K*. Journal of Applied Physics, 1991, **70**(2), p.846-854.

175. Jiang, Todd D. Krauss, and Louis E. Brus. *Electrostatic Force Microscopy Characterization of Trioctylphosphine Oxide Self-assembled Monolayers on Graphite*. 2000, **104**(50), p.11936-11941.

176. M. A. Thompson, *ArgusLab*. 2004. Available from: http://www.arguslab.com

177. J. J. Benitez, O. Rodriguez de la Fuente, I. Diez-Perez, F. Sanz, and M. Salmeron. *Dielectric properties of self-assembled layers of octadecylamine on mica in dry and humid environments*. 2005, **123**(10), p.104706.

178. Masashi Takahashi, Koichi Kobayashi, Kyo Takaoka, and Kazuo Tajima. *Structural Characterization of an Octadecylamine Langmuir-Blodgett Film Adsorbed with Methyl Orange*. Journal of Colloid and Interface Science, 1998, **203**(2), p.311-316.

179. London King's College. *Dr. Mark Green*. 2009 [cited 15/09/2009]; Available from: http://www.kcl.ac.uk/schools/pse/physics/people/academic/green/.

180. U. H. Pi, M. S. Jeong, J. H. Kim, H. Y. Yu, Chan Woo Park, H. Lee, and Sung-Yool Choi. *Current flow through different phases of dodecanethiol self-assembled monolayer*. Surface Science, 2005, **583**(1), p.88-93.

181. R. L. Whetten and R. C. Price. *Chemistry: Nano-Golden Order*. Science, 2007, **318**(5849), p.407-408.

182. P. D. Jadzinsky, G. Calero, C. J. Ackerson, D. A. Bushnell, and R. D. Kornberg. *Structure of a Thiol Monolayer-Protected Gold Nanoparticle at 1.1 A Resolution*. Science, 2007, **318**(5849), p.430-433.

183. Sigma-Aldrich. *182427 - Polystyrene Pellets*. 2009 [cited 02/08/2009]; Available from:

http://www.sigmaaldrich.com/catalog/ProductDetail.do?lang=en&N4=182427|ALDRICH&N5=SEARCH_CONCAT_PNO|BRAND_KEY&F=SPEC.

184. Sigma-Aldrich. *436224 - Poly(4-vinylphenol)*. 2009 [cited 02/08/2009]; Available from: http://www.sigmaaldrich.com/catalog/ProductDetail.do?lang=en&N4=436224|ALDRICH&N5=SEARCH_CONCAT_PNO|BRAND_KEY&F=SPEC.

185. Sigma-Aldrich. *164984 - 8-Hydroxyquinoline*. 2009 [cited 02/08/2009]; Available from: http://www.sigmaaldrich.com/catalog/ProductDetail.do?lang=en&N4=164984|ALDRICH&N5=SEARCH_CONCAT_PNO|BRAND_KEY&F=SPEC.

186. D. R. Lide, *CRC Handbook of Chemistry and Physics.* 89th Edition ed. 2008: Taylor and Francis Ltd.

Appendices

9.1. Appendix A – Polymer and Chemical Acronyms:

8HQ.....8-hydroxyquinoline

AIDCN.....2-amino-4,5-imidazoledicarbonitrile

DDQ.....2,3-dichloro-5-6dicyano-1,4-benzoquinone

MDCPAC.....poly(methylmethacrylate-co-9-anthracenyl-methylmethacrylate)

P3HT.....poly(3-hexylthiophene)

PCm .....(4-cyano-2,4,4-trimethyl-2-methylsulfanylthiocarbonylsulfanyl-poly(butyric acid 1-adamantan-1-yl-1-methyl-ethyl ester))

PEDOT.....poly(3,4-ethylenedioxythiophene)

PS.....polystyrene

PTFE.....polytetrafluoroethylene

PVA .....polyvinyl alcohol

PVP.....poly-4-vinylphenol

PVK .....poly(n-vinylcarbazole)

TAPA.....(+)-2-(2,4,5,7-tetranitro-9-fluorenylideneaminooxy) propionic acid

9.2. Appendix B – List of Acronyms

1L-OBD ..... 1-Layer Organic Bistable Devices
3L-OBD ..... 3-Layer Organic Bistable Devices
AC ..... Alternating Current
AFM ..... Atomic Force Microscope/Microscopy
c-AFM ..... Conducting Atomic Force Microscopy
CD-RW ..... Rewritable Compact Disc
CNT ..... Carbon Nanotube
CS-AFM ..... Current Sensing Atomic Force Microscopy
CVD ..... Chemical Vapour Deposition
DRAM ..... Dynamic Random Access Memory
DUT ..... Device Under Test
DVD-RW ..... Rewritable Digital Versatile Disc
EDX ..... Energy Dispersive X-ray Analysis
EFM ..... Electrical Force Microscopy
FeRAM ..... Ferroelectric Random Access Memory
HDD ..... Hard Disc Drive
IC ..... Integrated Circuit
ITRS ..... International Technology Roadmap for Semiconductors
I-V ..... Current-Voltage
LB ..... Langmuir-Blodgett
LCD ..... Liquid Crystal Display
LED ..... Light Emitting Diode
MIM ..... Metal-Insulator-Metal
MIS ..... Metal-Insulator-Semiconductor
MRAM ..... Magnetoresistive Random Access Memory
NDR ..... Negative Differential Resistance
NRAM ..... Nano Random Access Memory
OLED ..... Organic Light-Emitting Diode
OMD ..... Organic Memory Device
PCB ..... Printed Circuit Board
PCRAM ..... Phase-Change Random Access Memory
PMD ..... Polymer Memory Device
PROM ..... Programmable Read Only Memories

RPM ..... Revolutions Per Minute
RRAM ..... Resistive Random Access Memory
RWE ..... *Read*, *Write* and *Erase* Cycles
SCLC ..... Space Charge Limited Conduction
SEM ..... Scanning Electron Microscope/Microscopy
SPM ..... Scanning Probe Microscope/Microscopy
STM ..... Scanning Tunneling Microscope/Microscopy
SV ..... Simmons and Verderber
TEM ..... Transmission Electron Microscope/Microscopy
TMV ..... Tobacco Mosaic Virus
UHV-STM ..... Ultra-High-Vacuum Scanning Tunneling Microscope
WORM ..... Write Once, Read Many Times

9.3. Appendix C – Physical Constants

Values sourced from CODATA recommended values of the fundamental physical constants: 2006 [173] unless otherwise stated.

N_A ..... Avagadro Constant ..... $6.022\ 141 \times 10^{23}$ mol^{-1}

k ..... Boltzmann Constant ..... $1.380\ 650 \times 10^{-5}$ J K^{-1}

e ..... Elementary Charge ..... $1.602\ 176 \times 10^{-19}$ C

h ..... Planck Constant ..... $6.626\ 069 \times 10^{-34}$ J·s

$\hbar$ ..... Reduced Planck Constant ..... $1.054\ 572 \times 10^{-34}$ J·s

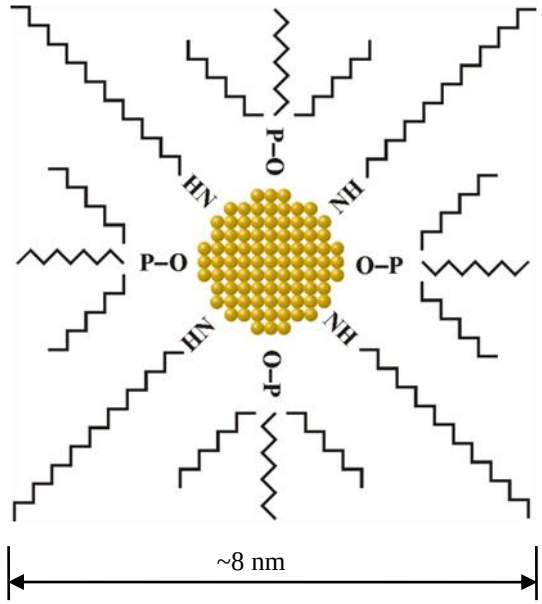
n_i ..... Silicon Intrinsic Carrier Concentration [174] ..... 1.00×10^{10} cm^{-3}

E_g ..... Silicon Band-gap ..... 1.12 eV

ε_o ..... Vacuum Permittivity ..... $8.854\ 188 \times 10^{-12}$ F m^{-1}

9.4. Appendix D – Chemical Structures of Key Materials.

Type-I Gold Nanoparticles:



Capping ligands:

Tri-n-octylphosphene oxide:

Dielectric constant ~2.5 [175]

Molecule length ~1.3 nm from simulations in ArgusLab [176]

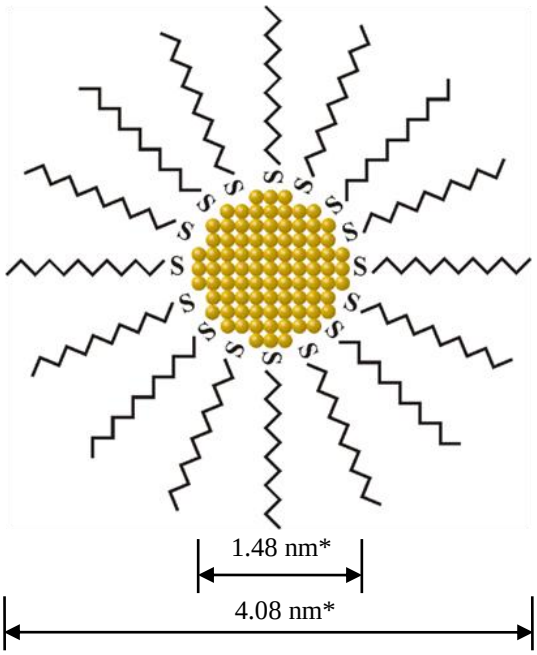
Octadecylamine:

Dielectric constant ~2.0 [177]

Molecule length ~2.3 nm [177-178] and from simulations in ArgusLab [176]

Manufactured and supplied by Dr. Mark Green, King's College, London [179]

Type-II Gold Nanoparticles [155]:



Capping ligands:

Dodecanethiol:

Dielectric constant ~2.7 [149]

Molecule length ~1.3 nm [180] and from simulations in ArgusLab [176]

*For calculations involving the size of the nanoparticle core an assumption is made that the capping ligands are straight, and align themselves with the carbon chain away from the nanoparticle core. Recent work on the structure of gold nanoparticles suggests that this may not be the case, and chirality is possible [181-182]. Manufacturers TEM analysis [155] states that the mean nanoparticle size is 4.08 nm, however further TEM analysis has not taken place, so core size and size distribution is unknown. For calculations performed in this research a nanoparticle diameter of 4.08 nm and capping ligand length of 1.3 nm will be assumed throughout, resulting in a core diameter of 1.48 nm.

Type-II Gold Nanoparticle Certificate of Analysis (Batch 04918MH) [155]:

Certificate of Analysis

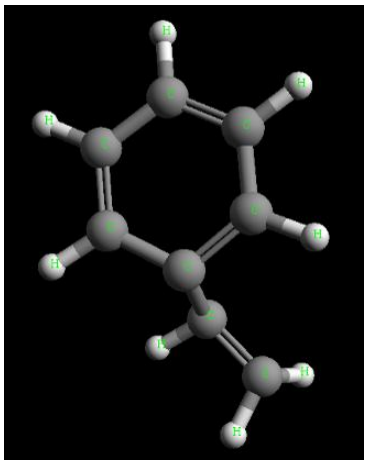
SIGMA-ALDRICH

Product Name	Dodecanethiol functionalized gold nanoparticles, 3-5 nm particle size (TEM), 2 % (w/v) in toluene
Product Number	660434
Product Brand	ALDRICH

TEST	**SPECIFICATION**	**LOT 04918MH RESULTS**
APPEARANCE	DARK RED TO BROWN LIQUID	DARK PURPLE LIQUID
INFRARED SPECTRUM		CONFORMS TO STRUCTURE.
ICP ASSAY	CONFIRMS GOLD COMPONENT	CONFIRMS GOLD COMPONENT
PARTICLE SIZE	4-6 NM (D90, DYNAMIC LIGHT SCATTERING)	MEAN DIAMETER: 4.08 NM* * SUPPLIER DATA
MEASUREMENTS	REVISED FEBRUARY 27, 2006 JLH	
QC RELEASE DATE		NOVEMBER 2007

Barbara Rajzer, Supervisor
Quality Control
Milwaukee, Wisconsin USA

Styrene Monomer Structure:



Polystyrene chemical formula: $[CH_2\text{-}CH\text{-}(C_6H_5)]_n$

Supplied by Sigma Aldrich, order code: 182427

Batch number: 16311DB

Molar mass of PS used ~280,000 [183]

Certificate of Analysis (Batch 16311DB):

Certificate of Analysis

SIGMA-ALDRICH

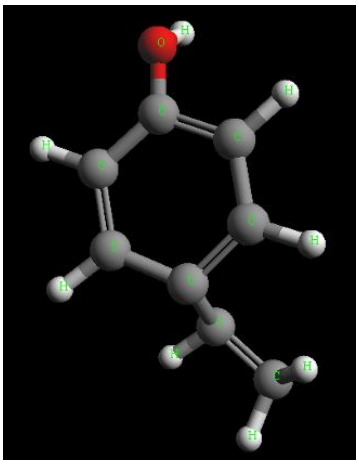
Product Name	Polystyrene, average M_w ~280,000 by GPC
Product Number	182427
Product Brand	ALDRICH
Molecular Formula	$[CH_2CH(C_6H_5)]_n$

TEST	SPECIFICATION	LOT 16311DB RESULTS
APPEARANCE	COLORLESS OR TRANSLUCENT PELLETS OR BEADS	COLORLESS PELLETS
INFRARED SPECTRUM	CONFORMS TO STRUCTURE	CONFORMS TO STRUCTURE AND STANDARD
MISCELLANEOUS ASSAYS	MELT INDEX: 2.8-3.8 G/10 MINUTES	MELT INDEX: 3.16 G/10 MINUTES
QC ACCEPTANCE DATE		APRIL 2003

Barbara Rajzer

Barbara Rajzer, Supervisor
Quality Control
Milwaukee, Wisconsin USA

4-Vinyl Phenol Monomer:



Poly-4-Vinyl Phenol chemical formula: $[CH_2\text{-}CH\text{-}(C_6H_4OH)]_n$

Supplied by Sigma Aldrich, order code: 436224

Batch number: 12027EB

Molar mass of PVP used ~25,000 [184]

Certificate of Analysis (Batch 12027EB):

Certificate of Analysis

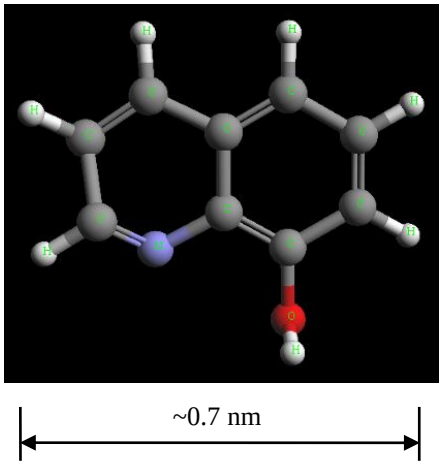
SIGMA-ALDRICH

Product Name	Poly(4-vinylphenol), average M_w ~25,000
Product Number	436224
Product Brand	ALDRICH
Molecular Formula	$[CH_2CH(C_6H_4OH)]_n$

TEST	SPECIFICATION	LOT 12027EB RESULTS
APPEARANCE	OFF-WHITE TO BEIGE OR TAN POWDER	LIGHT TAN POWDER
INFRARED SPECTRUM	CONFORMS TO STRUCTURE	CONFORMS TO STRUCTURE AND STANDARD
MOLECULAR WEIGHT DETERMINATION	CA. 20,000 (GPC)	AVERAGE MW: 21,000 (GPC)
TITRATION	TYPICALLY <5% H2O (WITH "KARL FISCHER"	< 2.0 % H2O (WITH "KARL FISCHER" REAGENT)
QC ACCEPTANCE DATE		MAY 2003

Barbara Rajzer, Supervisor
Quality Control
Milwaukee, Wisconsin USA

8-Hydroxyquinoline:



8-Hydroxyquinoline chemical formula: C_9H_7NO

Supplied by Sigma Aldrich, order code: 164984

Batch number: S25608-494 (Certificate of analysis unavailable).

Molar mass of 8HQ = 145.16 [185]

9.5. Appendix E – Supplementary Polystyrene Optimisation Data.

Dependence of the final film thickness on the spread speed can be seen in Figure 9.1. Spread speeds ranging from 200 – 1000rpm were investigated. Other parameters were kept constant at 4000 rpm final spin speed and 25 mg ml^{-1} polystyrene concentration.

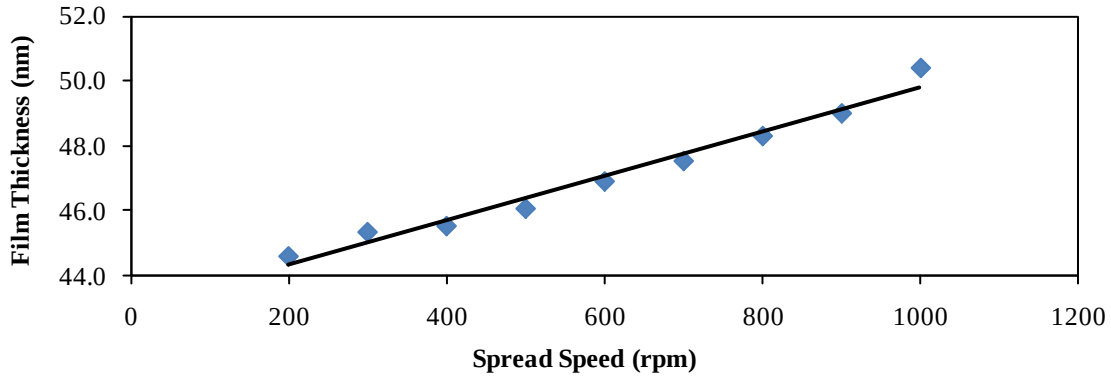


Figure 9.1 Final film thickness vs. spread speed. Black line shows linear best fit.

Figure 9.2 shows the effect of static vs. dynamic spin-coating. Films deposited via dynamic spin-coating are ~10% thinner on average than those deposited via static spin-coating. Spread speed was a constant 500rpm throughout and 35mgml^{-1} polystyrene concentration was used.

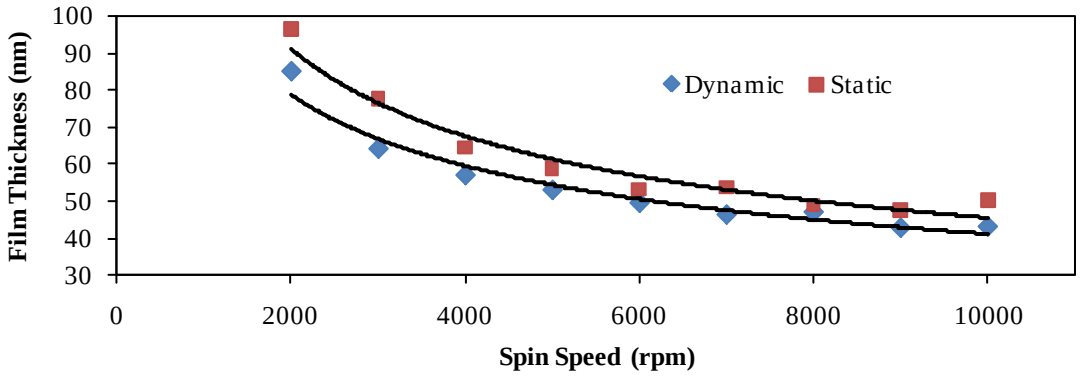


Figure 9.2 Static vs. dynamic spin-coating.

The polystyrene layer uniformity across the substrate is shown in Figure 9.3. 25 mm^2 p-type silicon was used as the substrate material. Measurements show a good uniformity across the bulk of the substrate with the main edge effects being concentrated in the outmost corners of the substrate.

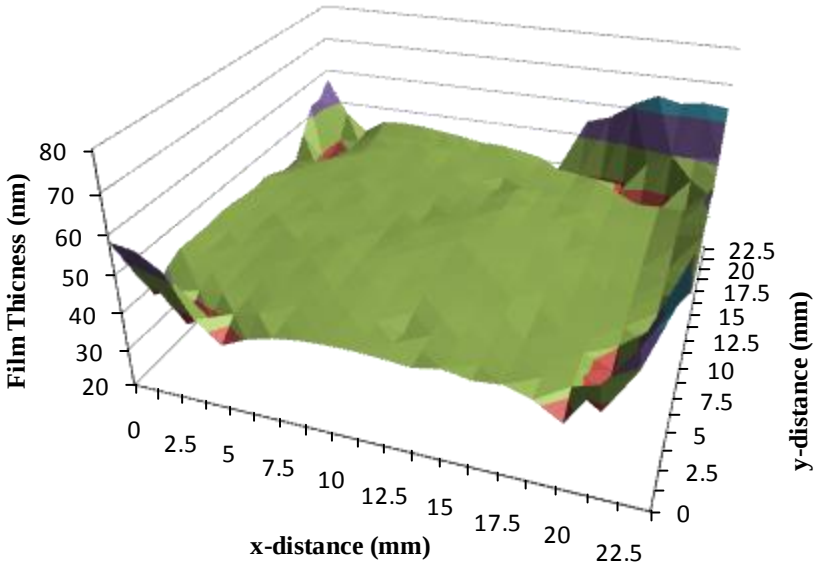
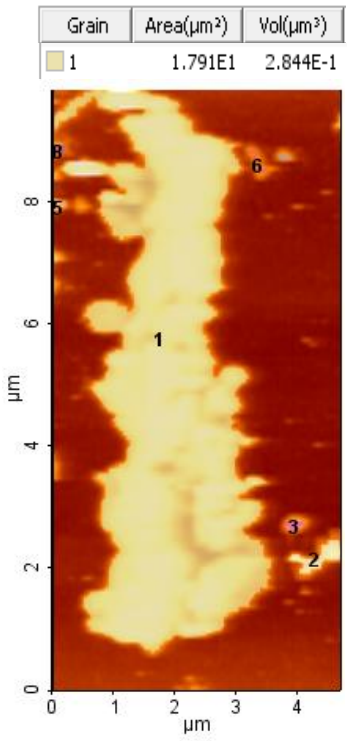


Figure 9.3 Polystyrene layer uniformity.

9.6. Appendix F – Supplemental Calculations.

9.6.1. Appendix F1 – Nanoparticle Island Volume and Capacitance Estimation



Volume of 4.08 nm diameter nanoparticle:

$= {}^{4}/_{3} \times \pi \times 2.04^3 = 35.56\ \text{nm}^3$

$C_{\text{Total}} = C_{NP} \times$ Number of nanoparticles

$$C_{\text{Total}} = \frac{2.9\text{x}10^{-19} \times 2.84\text{x}10^{8}}{35.56}$$

$C_{\text{Total}} = 2.32\text{x}10^{-12}$ F = 2.32 pF

$$\tau = R_T C_{NP} \therefore R_T = \frac{750}{2.32\text{x}10^{-12}} = 3.24\text{x}10^{14}\,\Omega$$

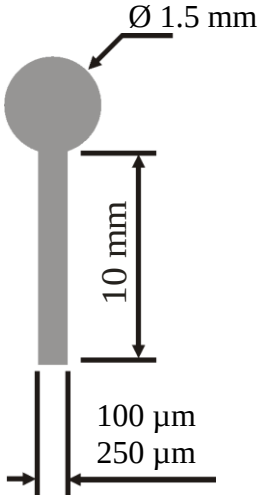
Resistance 100 nm SiO_2 for area under the island:

$$R = \frac{\rho l}{A} = \frac{1.0\text{x}10^{12} \times 100\text{x}10^{-9}}{1.791\text{x}10^{-11}} = 5.6\text{x}10^{15}\,\Omega$$

Resistance 20 nm air gap separating island, assuming area of 1 µm x 20 nm. Resistivity of air = $4.0\text{x}10^{13}$ Ω·m [186]:

$$R = \frac{\rho l}{A} = \frac{4.0\text{x}10^{13} \times 20\text{x}10^{-9}}{2.0\text{x}10^{-14}} = 4.0\text{x}10^{19}\,\Omega$$

9.6.2. Appendix F2 – Break Junction Electrode Capacitance Estimation



100 µm electrode:

$A = \pi \times 0.75^2 + (0.1 + 10)\ \text{mm}^2$

$A = 2.767\text{x}10^{-6}\ \text{m}^2$, $\varepsilon_r = 6.7$, $d = 200\,\mu\text{m}$

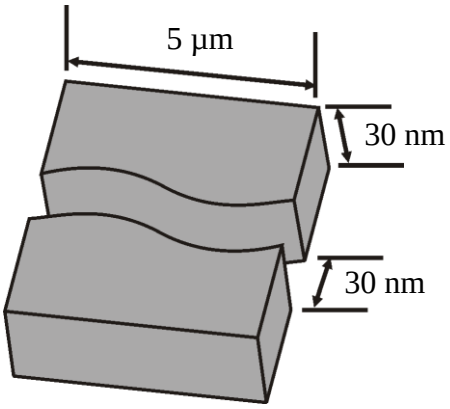
$$C = \frac{\varepsilon_r \varepsilon_0 A}{d} = \frac{6.7 \times 8.854\text{x}10^{-12} \times 2.767\text{x}10^{-6}}{200\text{x}10^{-6}}$$

$C = 8.2\text{x}10^{-13}$ F = 0.82 pF

250 µm electrode:

$C = 1.27\text{x}10^{-12}$ F = 1.27 pF

9.6.3. Appendix F3 – Break Junction Capacitance Estimations



Volume of break junction:

$= 5000 \times 30 \times 30 = 4.5\text{x}10^{6}$ nm^3

Volume of 4.08 nm diameter nanoparticle:

$= {}^{4}/_{3} \times \pi \times 2.04^3 = 35.56$ nm^3

$C_{\text{Total}} = C_{NP} \times$ Number of nanoparticles

$$C_{\text{Total}} = \frac{2.9\text{x}10^{-19} \times 4.5\text{x}10^{6}}{35.56}$$

$C_{\text{Total}} = 3.67\text{x}10^{-14}$ F ≈ 0.037 pF

9.6.4. Appendix F4 – Nanoparticle and 8HQ Separation in Typical PMDs at PS/8HQ/Gold-NP Ratios of 12/4/4 by Weight

Distance between gold nanoparticles:

Density of gold = 19.3 g·cm^{-3} = $1.93\text{x}10^{-17}$ mg·nm^3

Dodecanethiol density = 0.84 g·cm^{-3} = $8.4\text{x}10^{-19}$ mg·nm^3

Density of polystyrene = 1.047 g·cm^{-3} = $1.047\text{x}10^{-18}$ mg·nm^3

Volume of one memory cell in nanometres (1 mm^2 x 50 nm PS thickness):

$= (1\text{x}10^{6})^2 \times 50 = 5\text{x}10^{13}$ nm^3

Mass of PS in one memory cell:

$= 5\text{x}10^{13} \times 1.047\text{x}10^{-18} =$ <u>$5.24\ \text{x}10^{-5}$ mg</u>

Volume of 1.48 nm diameter nanoparticle core:

$= {}^{4}/_{3} \times \pi \times 0.74^3 = 1.70$ nm^3

Volume of 4.08 nm diameter nanoparticle shell:

$= {}^{4}/_{3} \times \pi \times 2.04^3 - 1.70 = 33.86$ nm^3

$\therefore$ mass of one nanoparticle = $(33.86 \times 8.4\text{x}10^{-19}) + (1.70 \times 1.93\text{x}10^{-17}) =$ <u>$6.13\text{x}10^{-17}$ mg</u>

Mass of nanoparticles in device = ${}^{5.24\text{x}10^{-5}}/_{3} = 1.75\text{x}10^{-5}$ mg

$\therefore$ number of NPs in one memory cell = ${}^{5.24\text{x}10^{-5}}/_{6.13\text{x}10^{-17}} = 2.86\text{x}10^{11}$ nanoparticles

$\therefore$ there is one nanoparticle per ${}^{5\text{x}10^{13}}/_{2.86\text{x}10^{11}} = 175$ nm^3 of memory cell

$\therefore$ distance between nanoparticle centres = $\sqrt[3]{175}$ = 5.6 nm

$\therefore$ estimated distance between nanoparticle shells = 5.6 – 4.08 = <u>1.52 nm</u>

Distance between 8HQ molecules:

Molar mass of 8HQ = 145.16 $g \cdot mol^{-1}$

$\therefore$ mass of one molecule = $145.16 / 6.0221412 \times 10^{23} = 2.41 \times 10^{-22}$ g = 2.41×10^{-19} mg

$\therefore$ number of 8HQ molecules in one memory cell = 7.24×10^{13} molecules

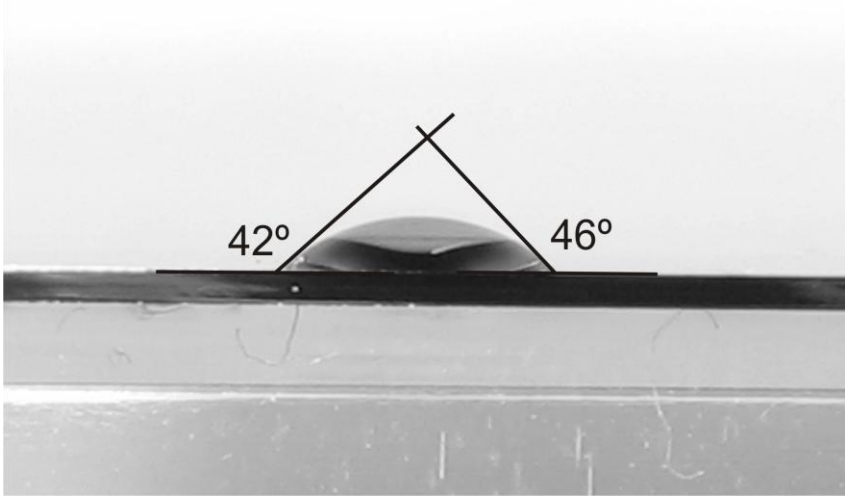
$\therefore$ there is one molecule per $5 \times 10^{13} / 7.24 \times 10^{13} = 0.69$ nm^3 of memory cell

$\therefore$ distance between molecule centres = $\sqrt[3]{0.69}$ = 0.88 nm

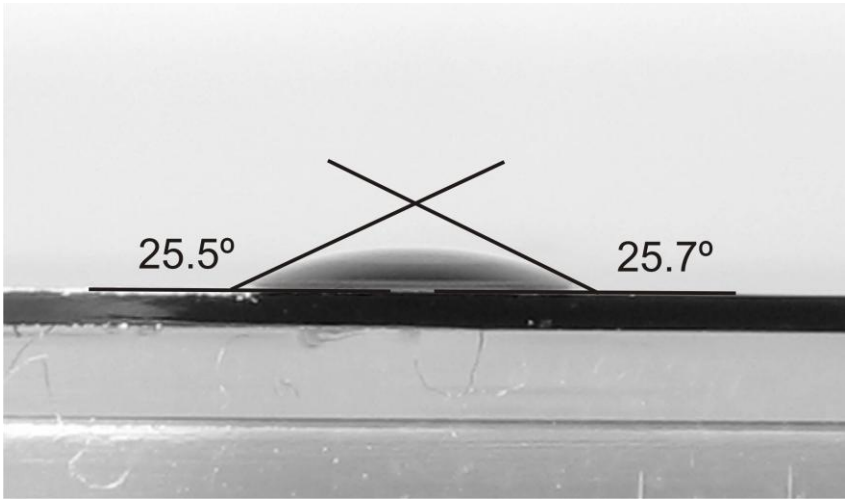
$\therefore$ estimated distance between molecules = 0.88 – 0.7 = <u>0.18 nm</u>

9.7. Appendix G – Contact Angle Images.

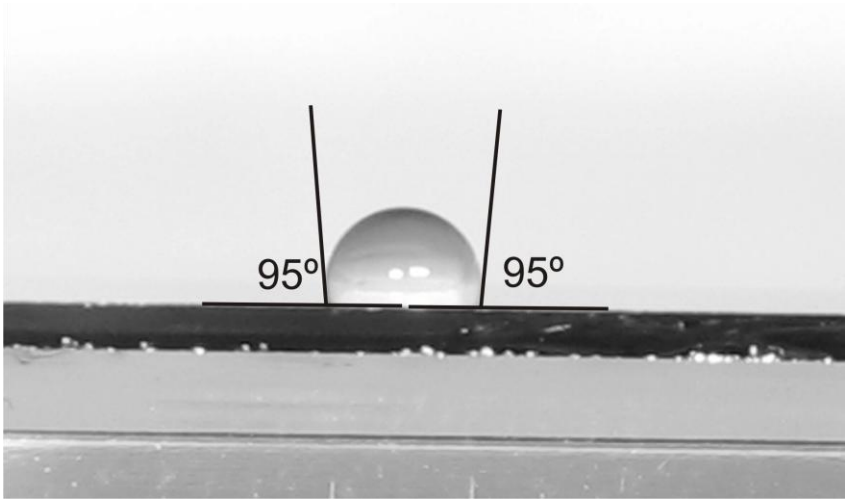
Cleaned Silicon – Average contact angle = 44°:



Silicon after silicon dioxide growth in nitric acid – Average contact angle = 25.6°:

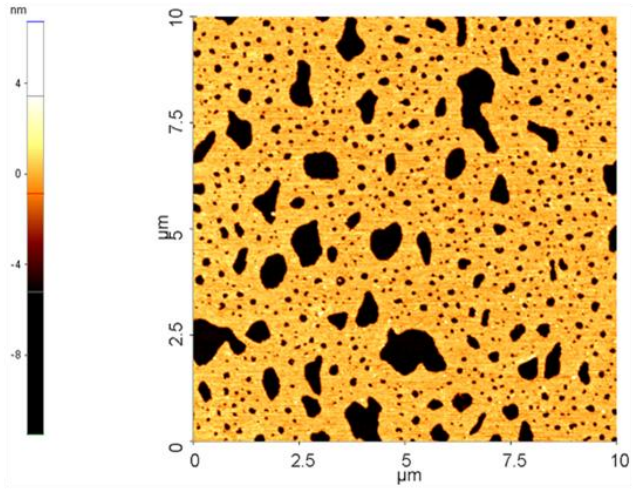


After silicon dioxide growth in nitric acid and silanisation – Average contact angle = 95°:



9.8. Appendix H – Supplemental AFM Substrate Images.

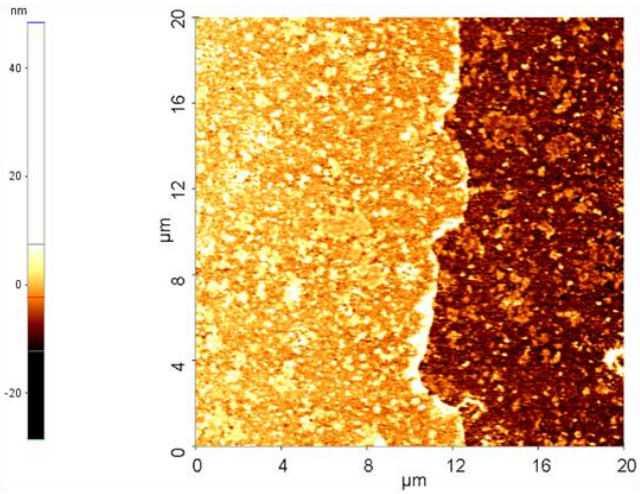
Type-II gold nanoparticles deposited on silicon dioxide substrate:



In all cases light areas correspond to areas of nanoparticle deposition.

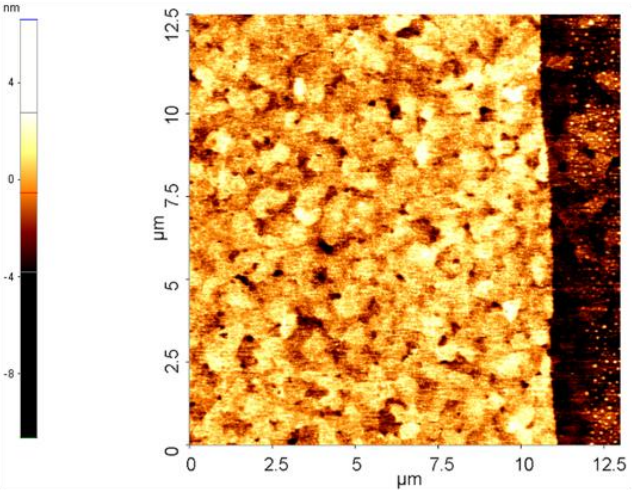
Substrate coverage ~85%

Type-II gold nanoparticles deposited on vacuum evaporated gold substrate:



Substrate coverage >99%

Type-II gold nanoparticles deposited on flame annealed gold substrate:

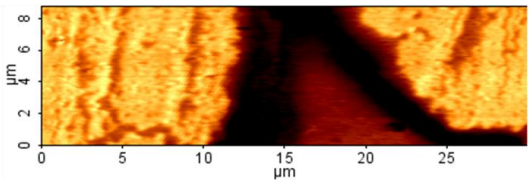


Substrate coverage >97%

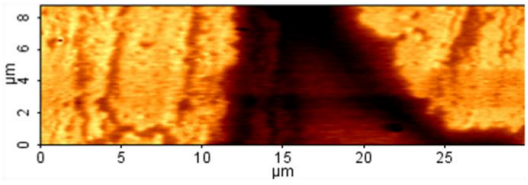
9.9. Appendix I – Gold Nanoparticle Charge Storage EFM images.

Read scans taken after applying +10V bias to electrodes, taken after:

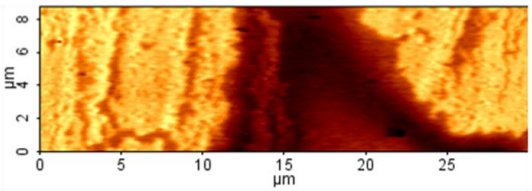
2 minutes:



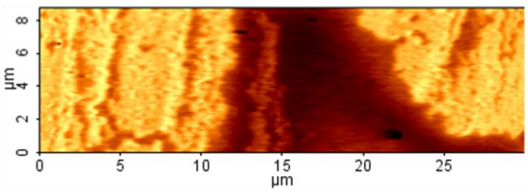
4 minutes:



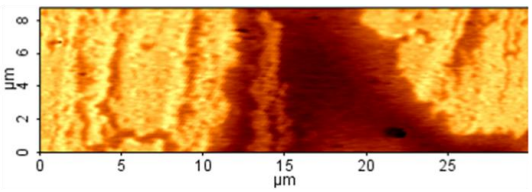
6 minutes:



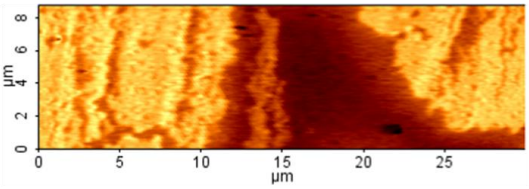
8 minutes:



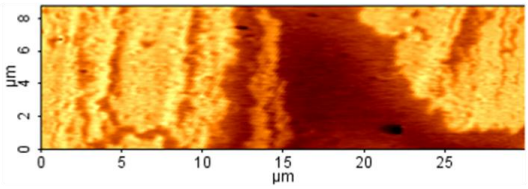
10 minutes:



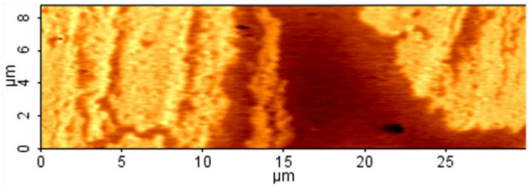
12 minutes:



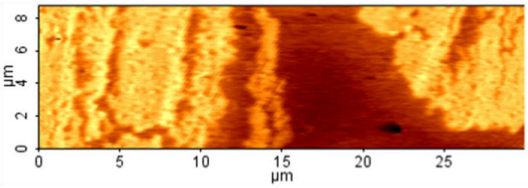
14 minutes:



16 minutes:

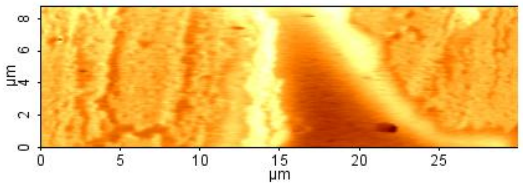


18 minutes:

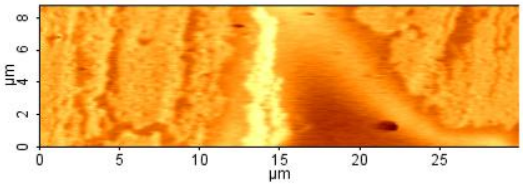


Read scans taken after applying -10V bias to electrodes, taken after:

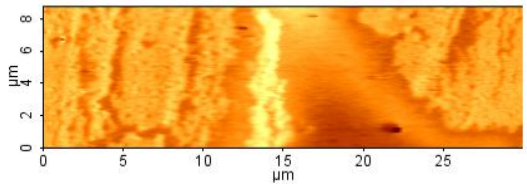
2 minutes:



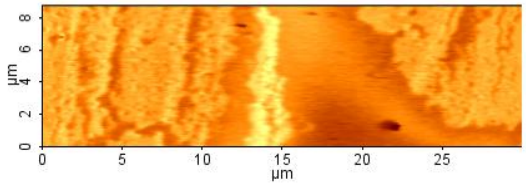
4 minutes:



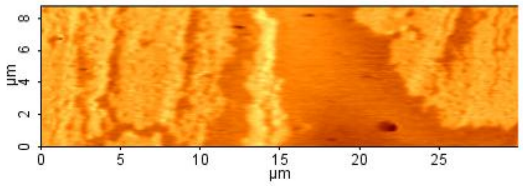
6 minutes:



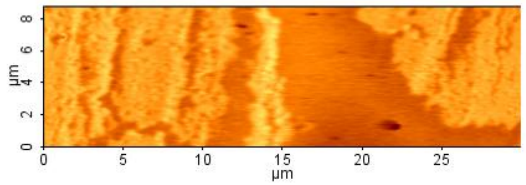
8 minutes:



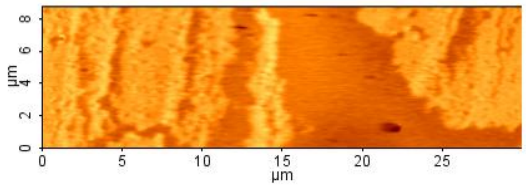
10 minutes:



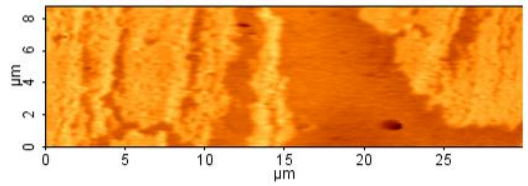
12 minutes:



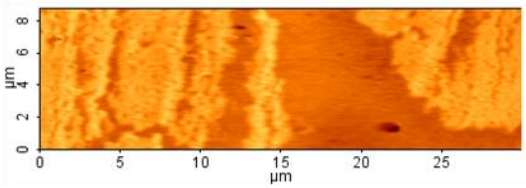
14 minutes:



16 minutes:



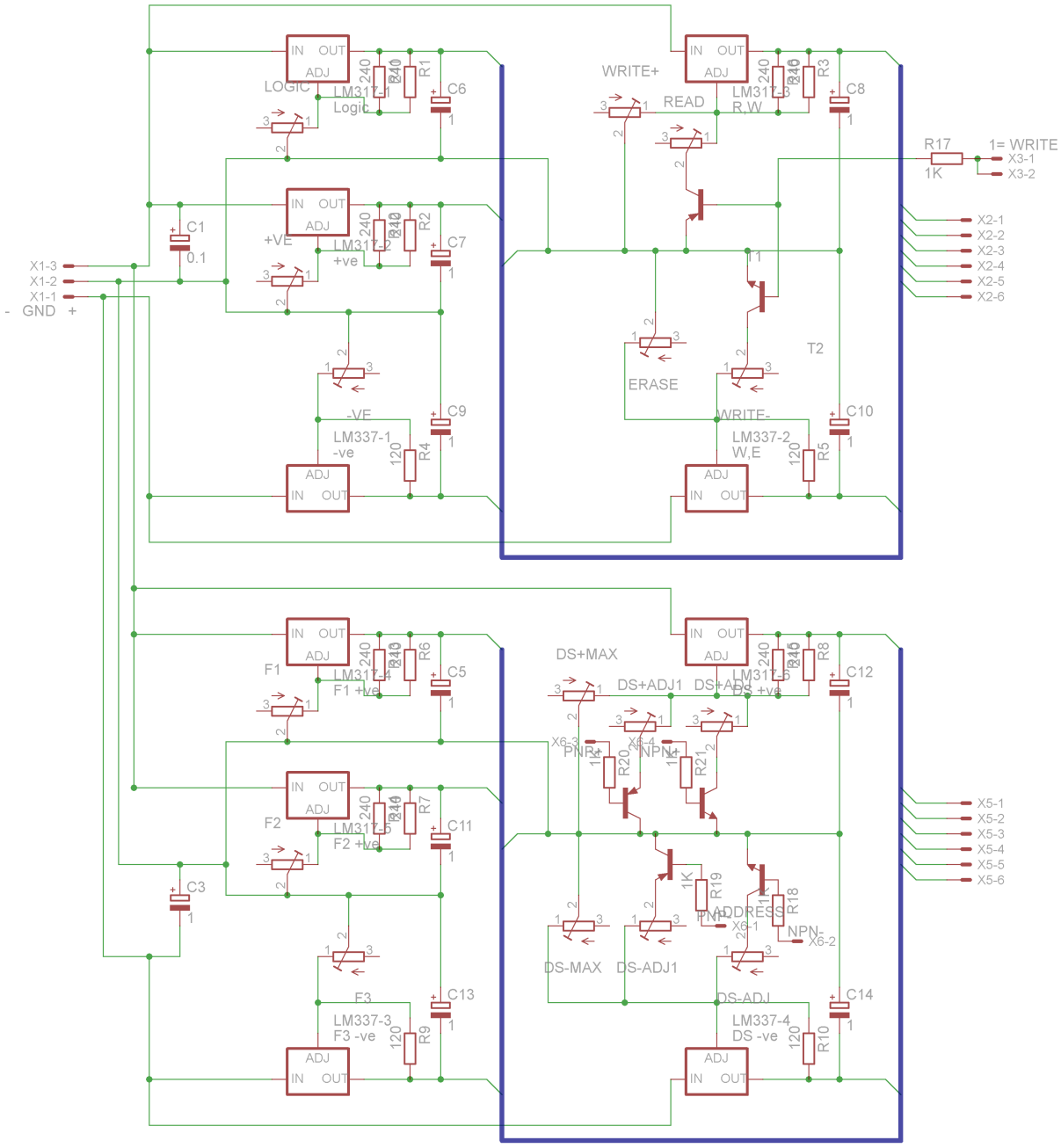
18 minutes:



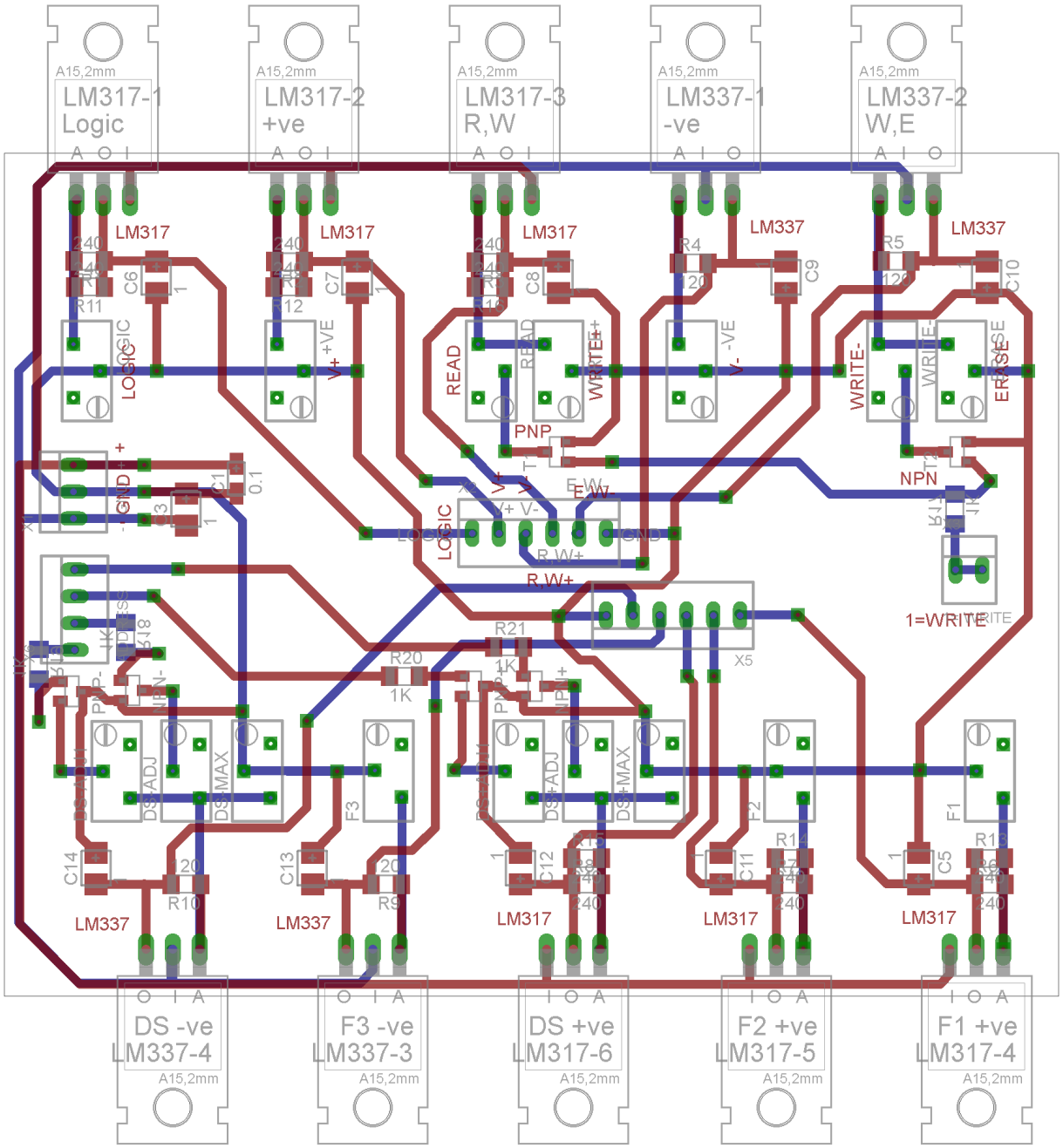
9.10. Appendix J – PMD Control and Decoder Circuit Schematics and PCB Layouts.

9.10.1. Appendix J1 – Voltage Supply

Voltage supply schematic:

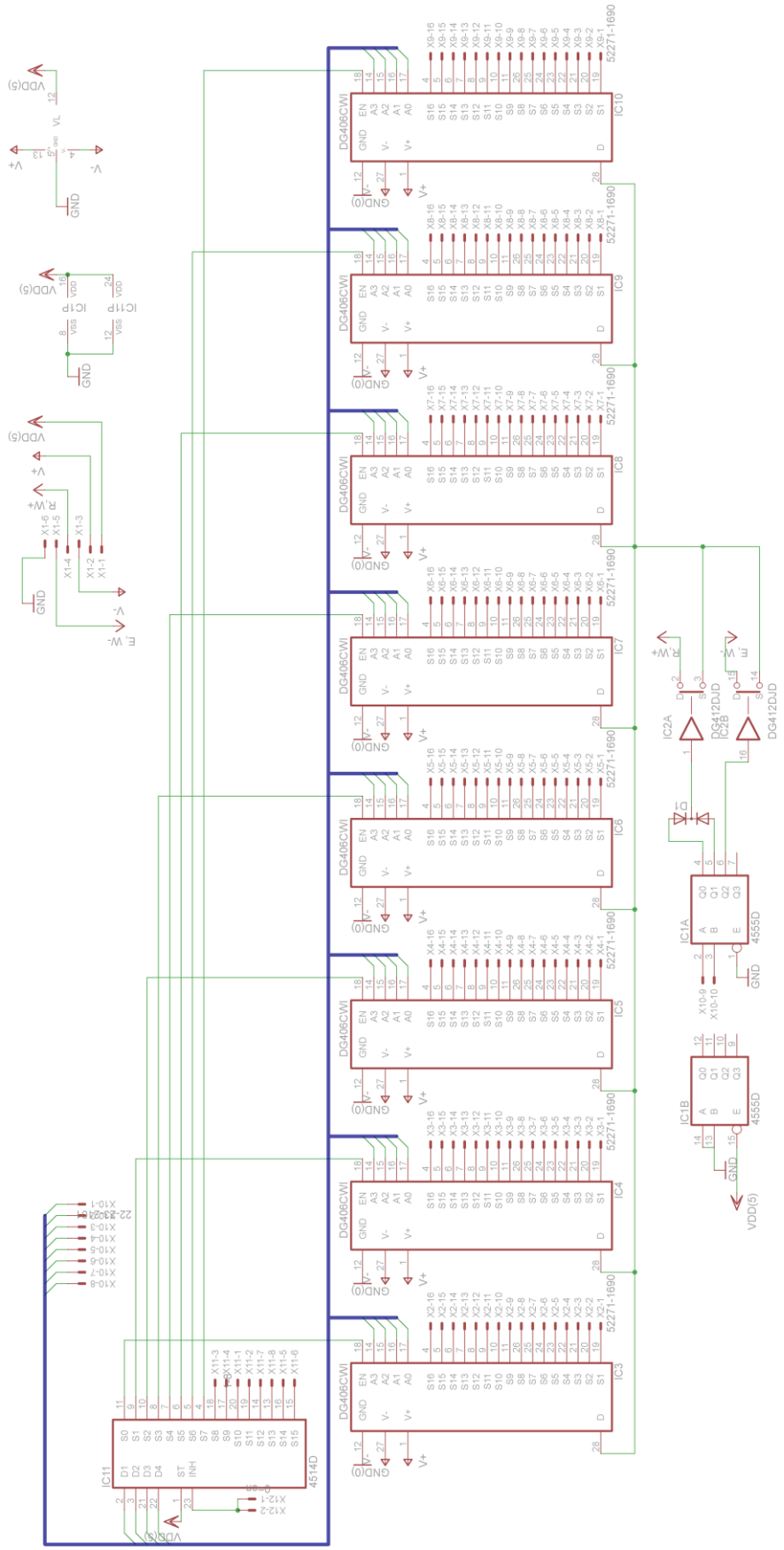


Voltage supply PCB layout. Top signal layer, red, bottom signal layer, blue:

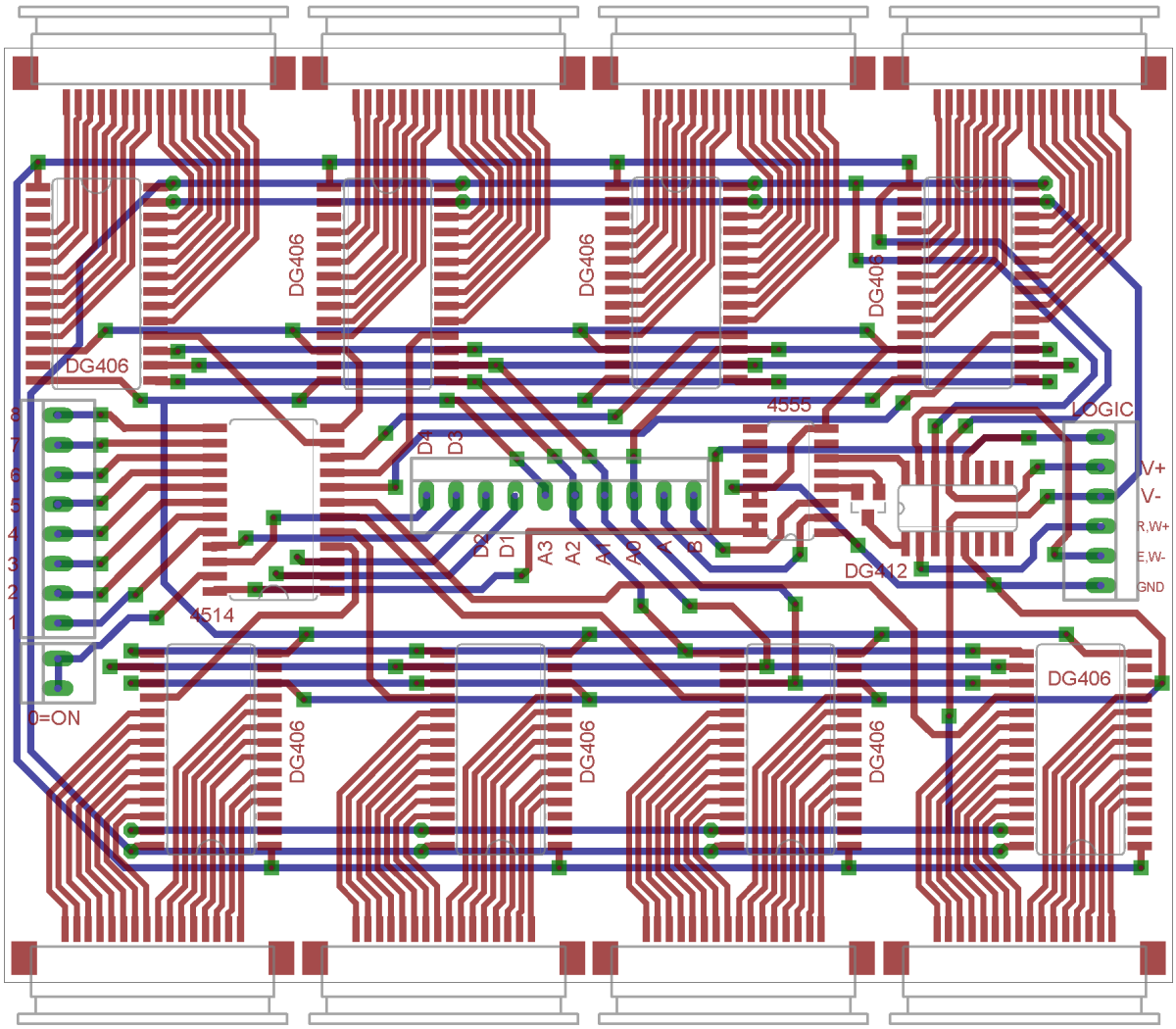


9.10.2. Appendix J2 – Row Address Decoder

Row address decoder schematic:

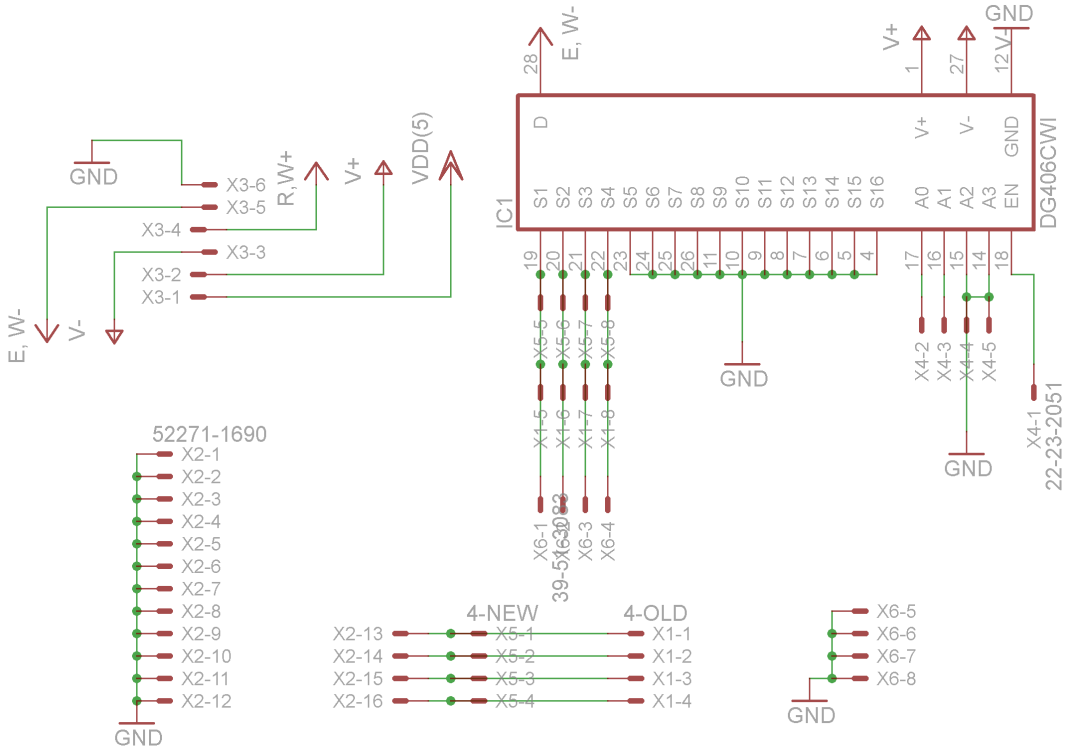


Row address decoder PCB layout. Top signal layer, red, bottom signal layer, blue:

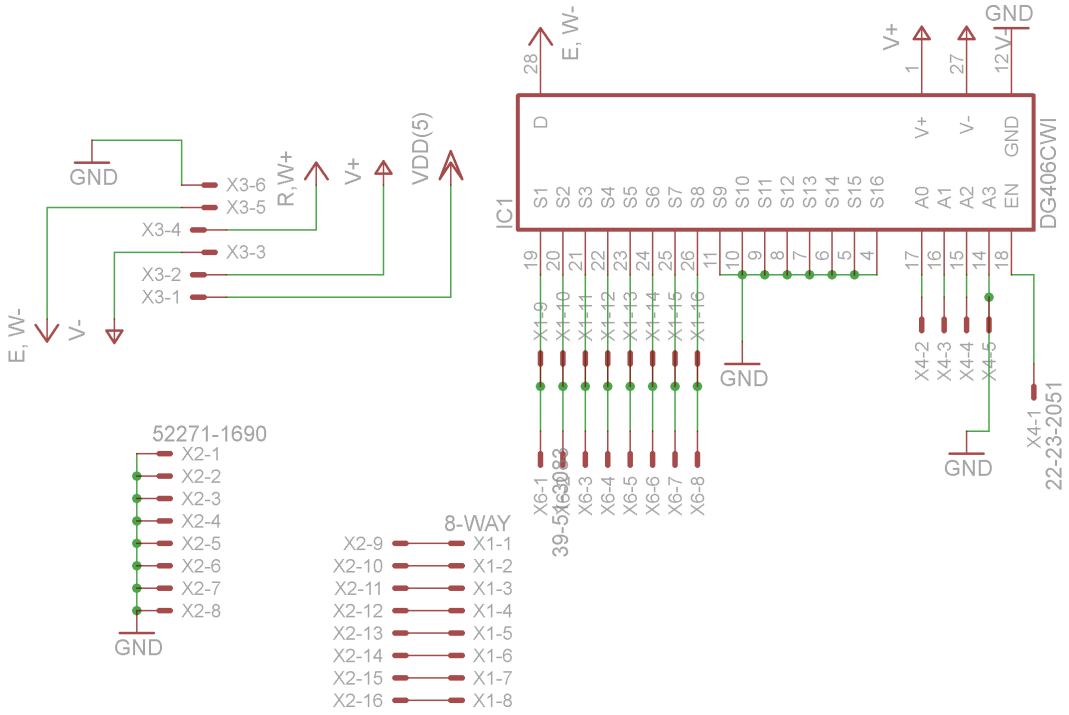


9.10.3. Appendix J3 – PMD Interface Board

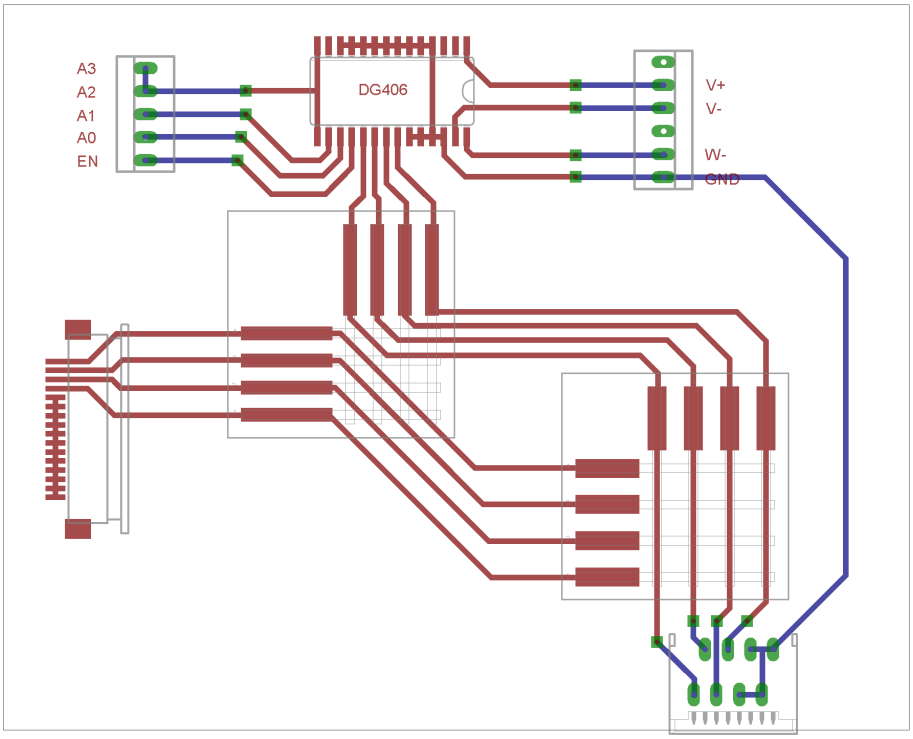
Interface board schematic for a 4-bit wide, 4 row PMD:



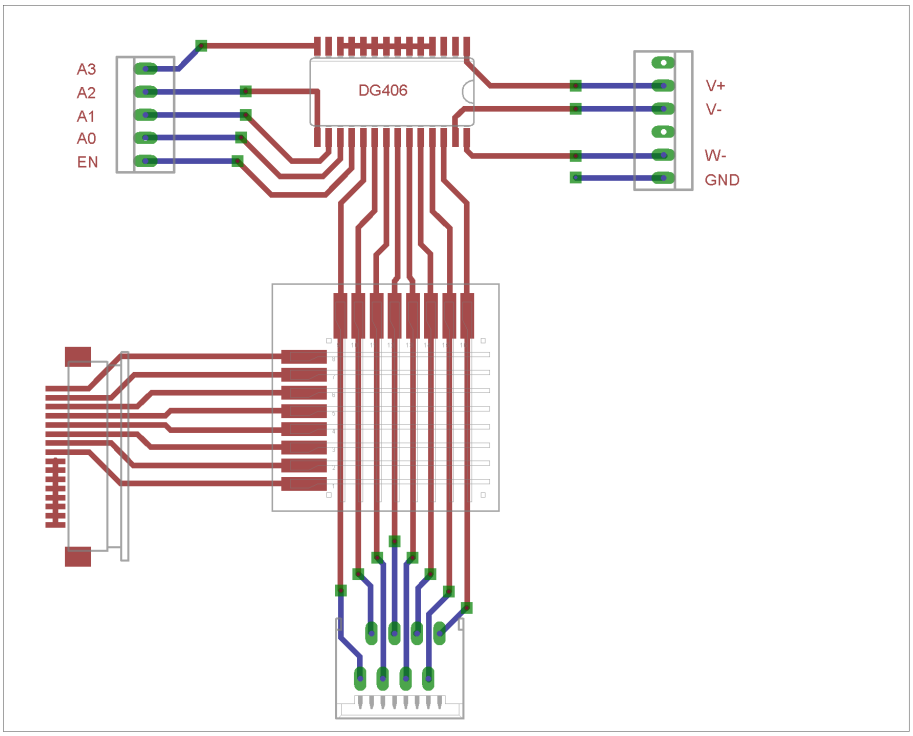
Interface board schematic for an 8-bit wide, 8 row PMD:



Interface board PCB for a 4-bit wide, 4-row PMD. Top signal layer, red, bottom signal layer, blue:

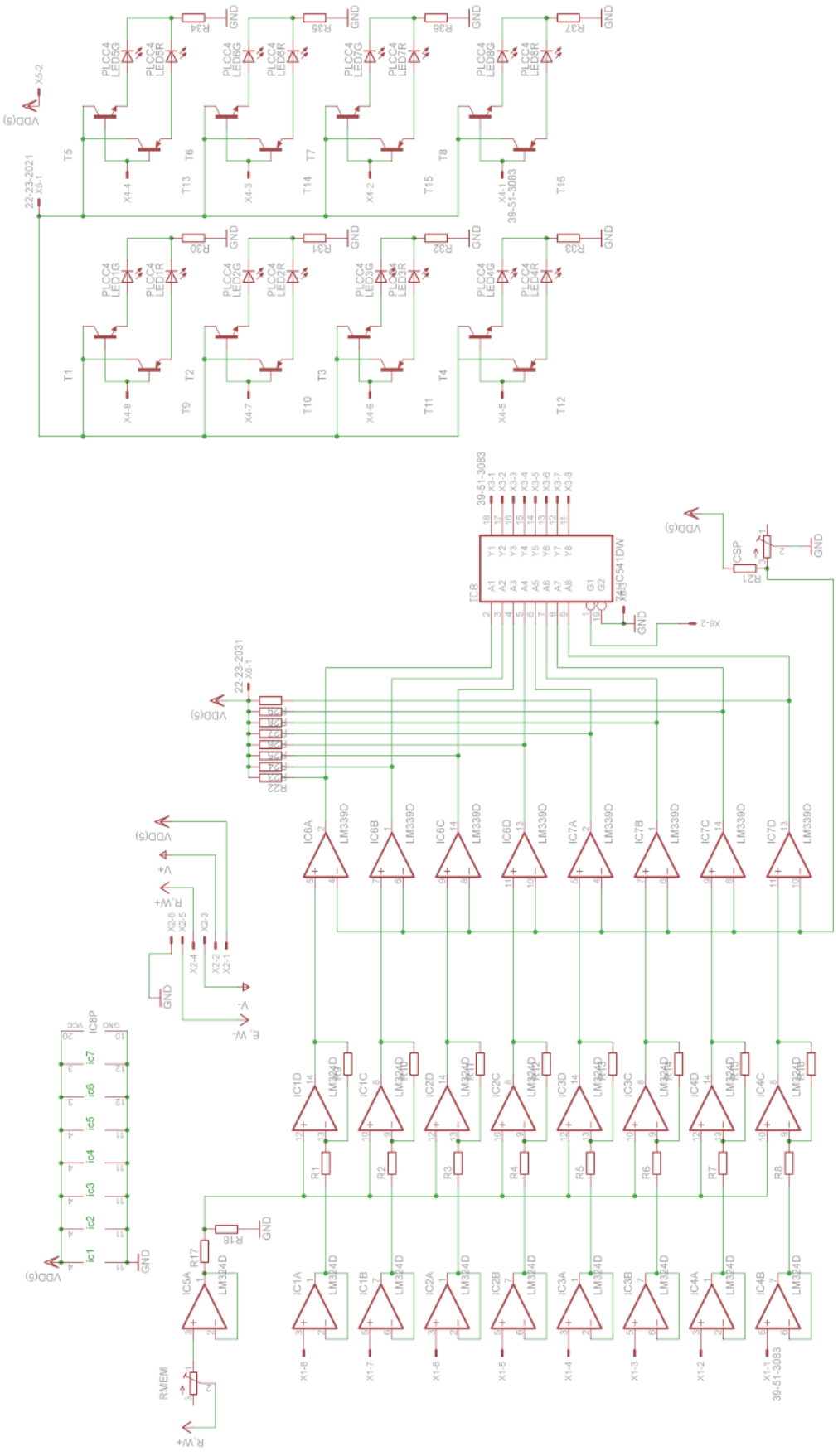


Interface board PCB for a 8-bit wide, 8-row PMD. Top signal layer, red, bottom signal layer, blue:

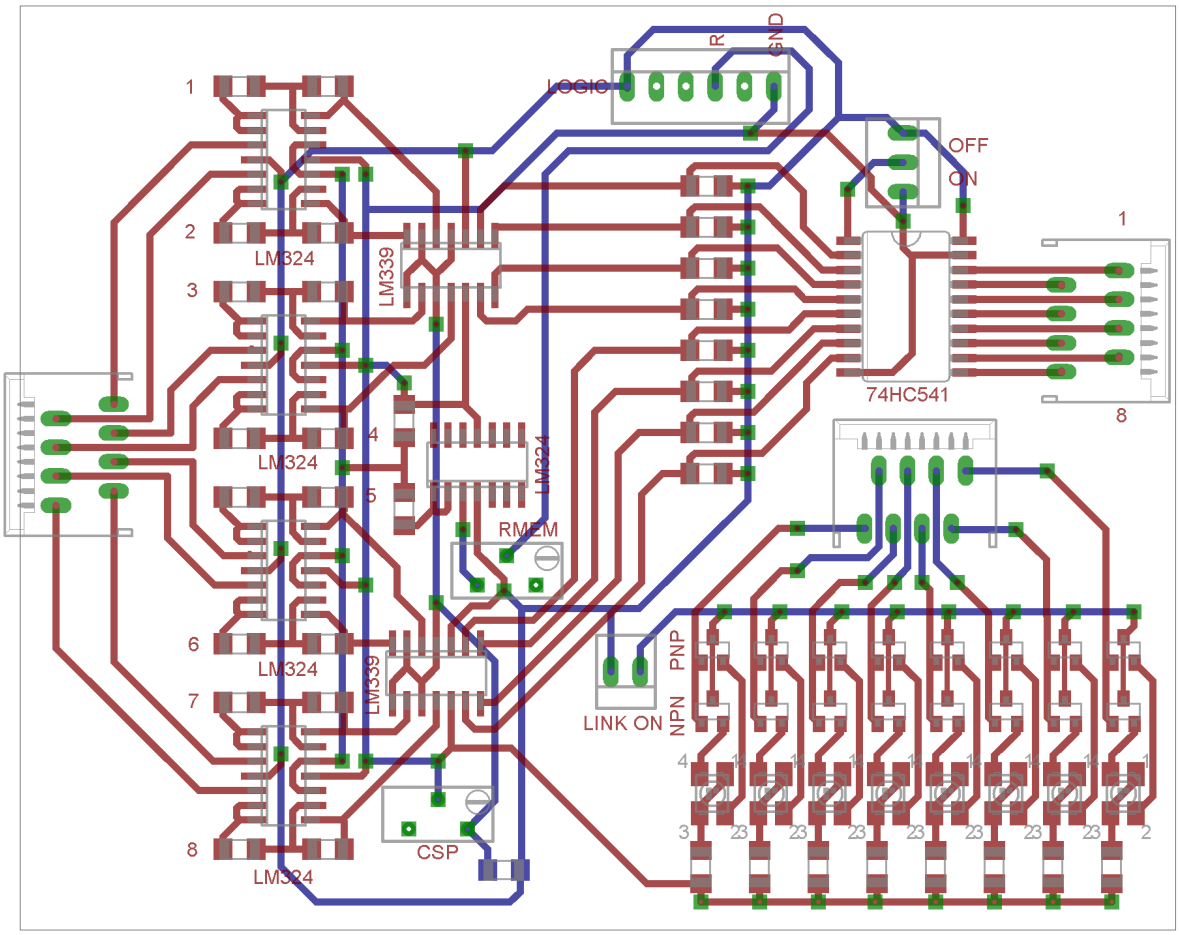


9.10.4. Appendix J4 – Output Decoders and Display.

Output decoder and display schematic:



Output decoders and display PCB layout. Top signal layer, red, bottom signal layer, blue:



"An education was a bit like a communicable sexual disease.
It made you unsuitable for a lot of jobs and then you had the urge to pass it on."
...Terry Pratchett